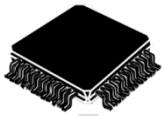
SPC1169 Datasheet

32-bit ARM Cortex-M4 based Auto-Grade MCU with 8 channel PWMs, 14 channel 13-bit ADC, 2 PGAs with Comparators

Features

- ARM 32-bit Cortex-M4 CPU Core with FPU
  - 100 MHz maximum frequency
- Memories
  - Up to 128 KB embedded flash
  - Up to 1 KB emulated EEPROM
  - Up to 32 KB on-chip SRAM
- Clock, reset and supply management
  - Single 3.3 V power supply
  - Optional 5V power supply to support 5V I/O
  - Sleep mode and stop mode for power saving
  - POR, Brown-out detector (BOD)
  - Crystal oscillator with both internal oscillator and external clock input support
  - Internal 32MHz factory-trimmed oscillator
  - Internal 32MHz backup-safety oscillator
  - PLL for CPU clock, maximum up to 100MHz
- 8-channel DMA controller
- 13-bit A/D converter (up to 14 channels)
  - As low as 200 ns conversion time
  - Single-ended and differential sampling
  - Open/short detection for safety
  - T-sensor
- Programmable gain amplifier (PGA)
  - One single-ended PGA with gain option:
    1, 2, 4, 8, 16, 32, 48, 64
  - One differential PGA with gain option:
    2, 4, 8, 16, 24, 32, 48, 64
  - Differential PGA supports -1.5V ~+2V input
- Analog comparator



LQFP48 (7 x 7 mm)

  - Two (one pair) high-speed comparators
  - Output with digital deglitch filter
  - Two DACs as reference
  - Out of range voltage protection
- Phase comparator
  - 3-phase input and 1 reference input channel
  - 3 dedicate phase comparators
- One D2S (Differential to single-ended) buffer
- Monitoring ADC (13-bit)
  - Monitor critical voltages
- PWM
  - Four enhanced PWM modules
  - 8 PWM outputs in total
  - Flexible waveform generation with phase lead/lag control
  - All events can trigger ADC conversion
- Up to 38 GPIO Pins
  - Configurable pull-up/pull-down resistors
  - Programmable digital input deglitch filter
  - Up to 14 GPIO with 3.3V
  - Up to 24 GPIO with 5V
- Enhanced Capture Module (ECAP)
  - Flexible input capture pin
  - Four 32-bit capture registers
  - Capture and APWM mode selection
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
- 6 Timers

- Three 32-bit general-purpose timers
- Two 32-bit watchdog timers
- SysTick timer 24-bit down-counter

- Communication interfaces
  - UART (with LIN support) x 2, External LIN PHY required
  - SPI x 2
  - I2C x 1
  - CAN (with CANFD support) x 1
- Security Modules
  - 64-bit unique ID, CRC x 1
- Operating temperature
  - Junction temperature: -40 to +150 °C
  - Automotive AEC-Q100 Grade 1 class

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Revision History

Version	Date	Author	State	Changes
1	2020-05-31	H.Su	Outdated	1. Initial release.
2	2021-12-28	H.Su	Outdated	1. Update Features. 2. Update Figure 1-1. 3. Update Figure 3-1. 4. Add Section 2.3, Section 2.23 and Section 2.24. 5. Update Section 2.10, Section 2.21 and Section 2.22. 6. Update Section 5. 7. Update Table 6-1. 8. Update Table 3-1, modify the description for debug pins. 9. Add D2S buffer information and characteristics.
3	2022-07-08	H.Su	Outdated	1. Update Section 2.12. 2. Update symbols in Table 5-2, Table 5-3, Table 5-4 and Table 5-5. 3. Update Table 5-9. 4. Update Table 5-7. 5. Update Table 5-8. 6. Update Figure 5-1. 7. Update Section 5.5. 8. Update Conditions of parameter RPU and RPD in Table 5-3. 9. Update Conditions of parameter RPU and RPD in Table 5-4. 10. Update Conditions of parameter RPU and RPD in Table 5-5.
A/0	2022-11-30	H.Su	Outdated	1. Update Features. 2. Update Figure 1-1 and Figure 1-2. 3. Update Figure 3-1. 4. Update Table 3-1. 5. Update Figure 4-1. 6. Update Section 2.8. 7. Update Table 5-9. 8. Update Section 2.18 and Section 5.12, modify the information for Monitoring ADC. 9. Update the notes for BOOT pin usage. 10. Update Section 2.17, add SPI FIFO depth information. 11. Update Section 2.18, add notes for CAN wake-up function.
A/1	2023-01-09	H.Su	Outdated	1. Update Table 5-19, add GBW and SR parameter values.

Version	Date	Author	State	Changes
C/0	2025-02-07	J. Zhou	Outdated	1. Update pin 38. 2. Delete EPWR. 3. Add a description of the performance of the DAC to generate waveform. 4. Add Section 2.2. 5. Modify Section 7 to ordering information. 6. Update Table 5-19, add data at different gains. 7. Add Section 5.24. 8. Add Section 3.2. 9. Add Section 5.4. 10. Update Table 5-1, Table 5-2, Table 5-3, Table 5-4, Table 5-5. 11. Update Table 5-13, add Figure 5-3. 12. Modify Section 2.16 I2C. 13. Correct parameter signs.
C/1	2025-07-31	J. Zhou	Released	1. Update Figure 2-2. 2. Modify V_{OH} and V_{OL} in Table 5-3, Table 5-4, Table 5-5. 3. Modify f_{RCO} in Table 5-13.

Terms or abbreviations

Terms or abbreviations	Description
DPGA	Differential Programmable Gain Amplifier
SPGA	Single-ended Programmable Gain Amplifier
D2S	Differential to Single-ended

1 Device overview

The SPC1169 device from Spintrol is a highly integrated system-on-chip (SoC) microcontroller. The SPC1169 incorporates a 32-bit ARM Cortex-M4 high-performance processor with a software-programmable clock rate as high as 100 MHz, 32 KB SRAM, 128 KB embedded flash with up to 1 KB EEPROM emulated by extra 12 KB flash, and an extensive range of enhanced I/Os and peripherals. The device offers a 13-bit ADC, one differential PGA and one single-ended PGA, four enhanced PWMs, three general-purpose 32-bit timers, as well as standard and advanced communication interface: two UARTs with LIN support, two SPIs, one I2C and one CAN.

The SPC1169 can operates from a 2.97 to 3.63 V power supply with DVDD5 pin tied to DVDD33 pin. It is also optional to provide a 4.5 to 5 V power supply to DVDD5 pin to enable 5V I/O feature. The temperature range is from -40 °C to +150 °C. The package type is 48-pin LQFP.

The SPC1169 employs function safety features such as backup clocking scheme, WDT interrupt and reset, open/short detection and background critical voltage monitoring. All these features make the SPC1169 ideal for motor control in automotive application.

Figure 1-1 shows the functional block diagram for the SPC1169. Figure 1-2 shows the clock tree information.

Figure 1-1: SPC1169 block diagram

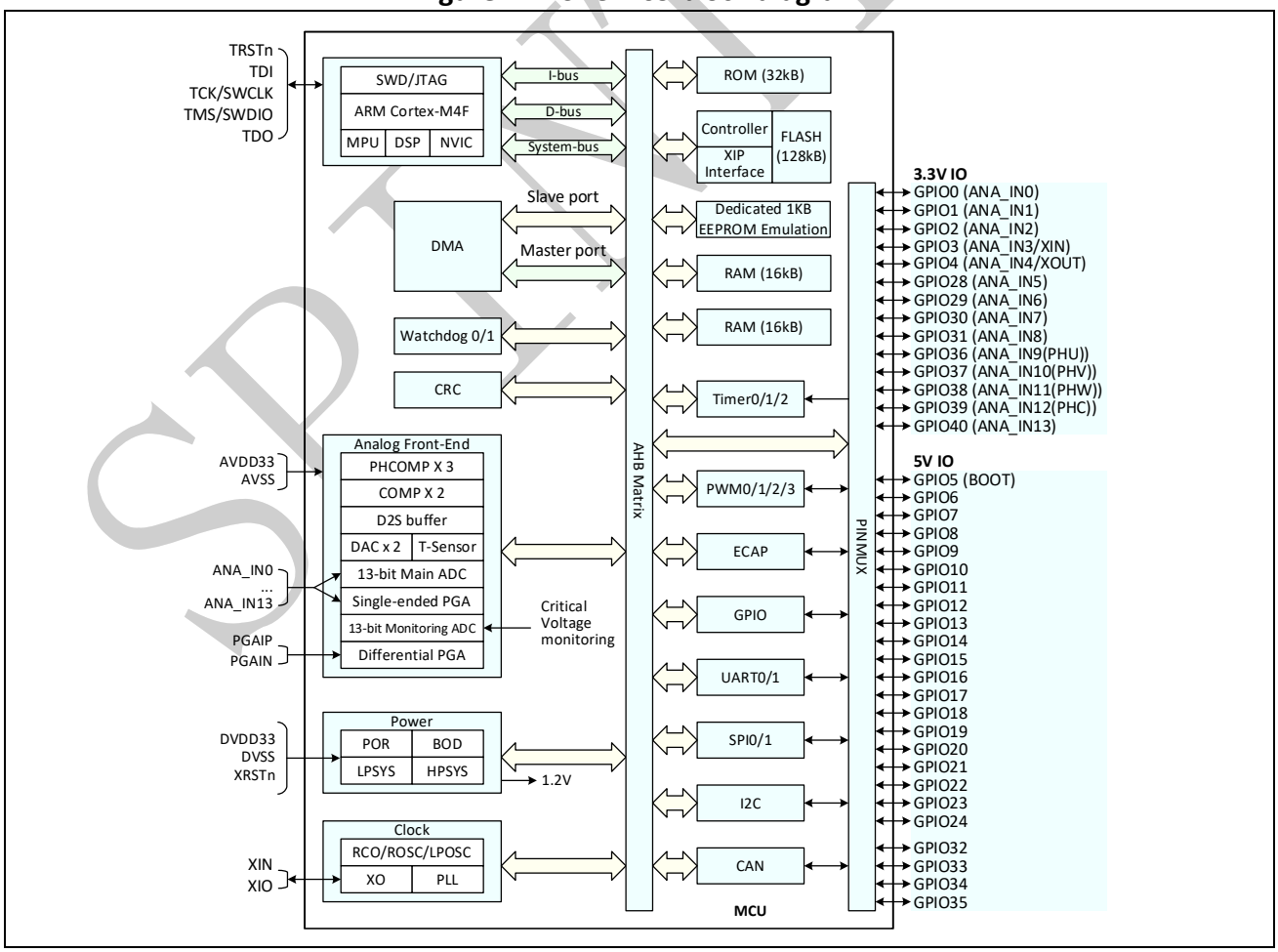
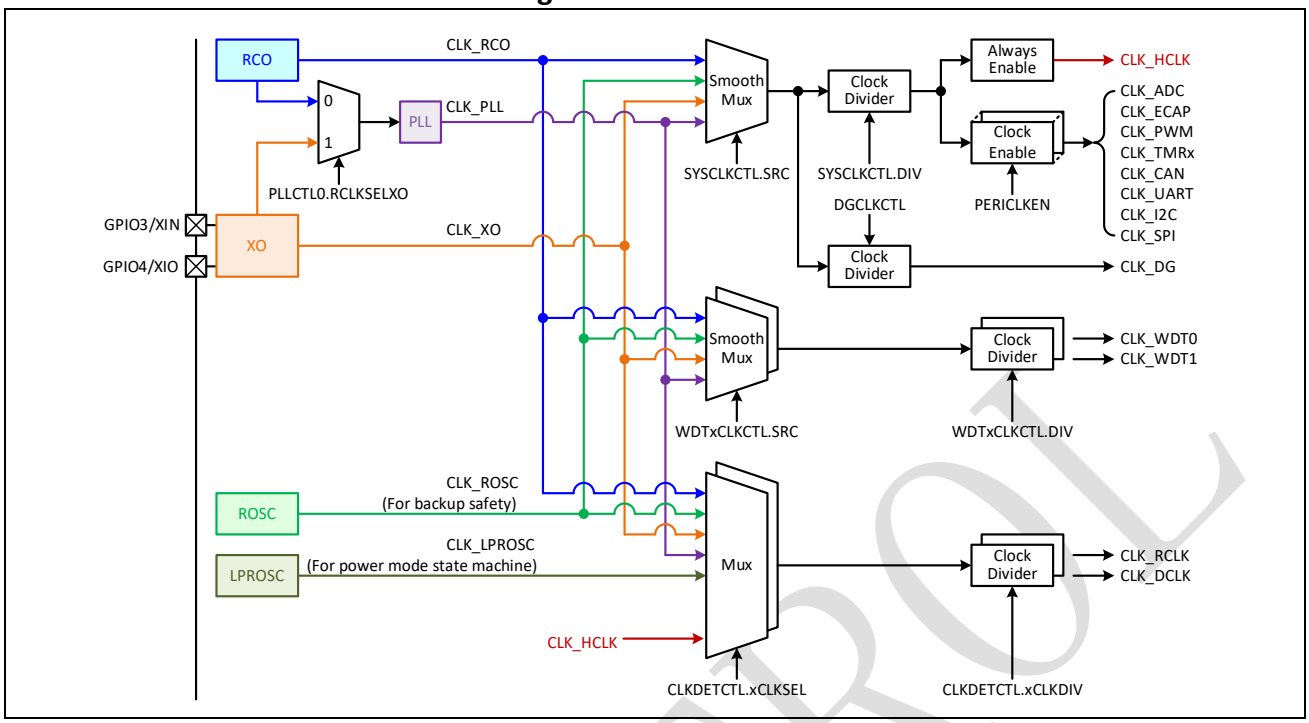


Figure 1-2: Clock tree



2 Feature descriptions

2.1 ARM Cortex-M4 core

The ARM Cortex-M4 processor has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The SPC1169 integrates a full-feature ARM Cortex-M4 core that can run up to 100MHz. Therefore, it is compatible with all ARM tools and software.

2.2 Serial line JTAG Debug Port (SWJ-DP)

The built-in ARM® SWJ-DP interface consists of a combination of JTAG and serial line debug ports. Based on the SWJ-DP interface, a serial line debug probe or a JTAG probe can be connected to the target. Debug ports can be disabled when SPC1169 enables certain security features.

Table 2-1: Debug interface Definition

Pin	serial line debug mode (turn off SWV[1])	Serial line debug mode (turn on SWV)	JTAG mode
GPIO15	function configured by software	function configured by software	TDI
GPIO16	function configured by software	SWV	TDO
GPIO17	SWD	SWD	TMS
GPIO18	SWCK	SWCK	TCK

[1] The purpose of GPIO16 is configured via bit 24 of the ARM® Cortex-M4F register (CoreDebug->DEMCR) at address 0xE000EDFC: 1 - SWV output; 0 -Functions configured by user software.

Note: In debug mode, the TRSTn must be set to a high level (5V).

2.3 Boot ROM

The Boot ROM contains boot code, Flash software library code and emulated EEPROM software library code. User can call Flash/ emulated EEPROM software library to operate Flash memory/emulated EEPROM directly.

2.4 Embedded SRAM

The SPC1169 has implemented 32 KB SRAM memory for code and data. The SRAM can be accessed (read/write) at CPU clock speed with 0 wait states.

2.5 Embedded Flash memory

Up to 128 KB of embedded Flash memory is available for storing programs and data. To enhance the lifetime and store critical data, another 12 KB Flash memory is used for EEPROM emulation to support up to 1 KB effective capacity.

2.6 Nested vectored interrupt controller (NVIC)

The SPC1169 embeds a nested vectored interrupt controller able to handle up to 54 mask-able interrupt channels (not including the 16 interrupt-lines of Cortex-M4) and 16 programmable priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Support for lazy-stacking
- Interrupt entry restored on interrupt exit with no instruction overhead

2.7 External interrupt/event controller

The SPC1169 provides a flexible external pin interrupt or event trigger mechanism. Any GPIO pin can be programmed as an external interrupt or event trigger source. In addition, any GPIO interrupt can be configured as edge-triggered or level-triggered.

2.8 Power supply and reset

The SPC1169 supports single power supply (3.3 V), which powers the IOs, internal voltage regulators and analog circuitry on chip. Supply ramp-up rate less than or equal 1.5x104 V/s.

The SPC1169 also supports dual power supply in which DVDD5 is 5V. It will enable fully 5V I/O capability for GPIO5 to GPIO24/GPIO36~GPIO40.

The SPC1169 has a global reset pin as well as an integrated power-on reset (POR) circuitry. The POR circuitry guarantees all power-up reset sequence requirements and makes the device easy to use.

2.9 Brown-out detector

The device features an embedded brown-out detector (BOD) that monitors the 3.3V/1.2V domain power supply and compare it to the programmable pre-set value. An interrupt or reset can be generate when voltage of the power domain is higher or drops below the pre-set value. The interrupt service routine then generates a warning message and/or put the MCU into a safe state. The BOD is enabled by software.

2.10 Clocks

System clock selection is performed on startup. The internal 32 MHz factory-trimmed oscillator is selected by default upon reset. An external oscillator can be selected by the user. When use external oscillator, there are two modes. One is supplying external clock directly and bypassing crystal oscillator. The other is using an external crystal and enable crystal oscillator (XO). The frequency of crystal can be selected within the range of 4 MHz to 32 MHz.

The device implements a fractional phase-lock loop (PLL) for high frequency clock generation. The PLL can take the internal 32MHz oscillator or external clock as the input reference clock. The output frequency covers from 25MHz to 100MHz.

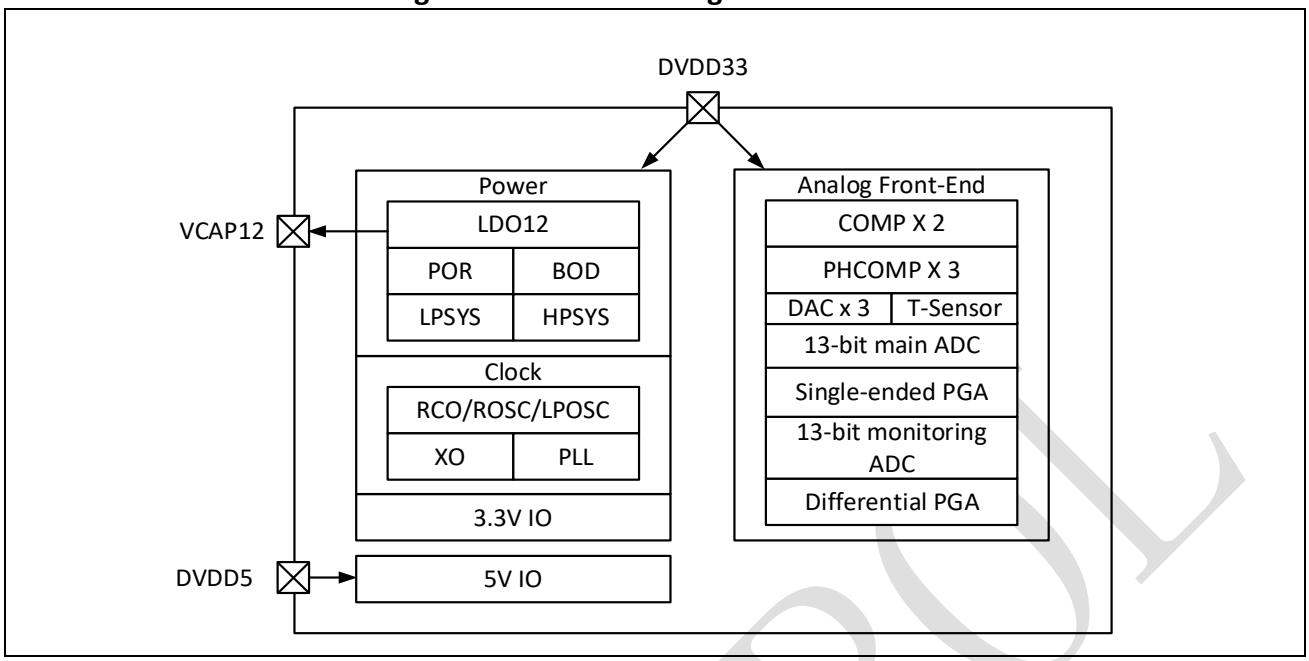
Several clock dividers allow the configuration of the AHB, and the peripherals frequency. The maximum allowed frequency is 50MHz for SPI and 100MHz for others. See Figure 1-2 for details on the clock tree. Special clock selection logic is designed so that the backup clock can take charge if current clock is missing. The 32MHz backup-safety oscillator makes the SPC1169 get rid of clock stuck.

2.11 Power mode

SPC1169 requires two power supplies, DVDD33 and DVDD5, where DVDD5 (5V) is only used for 5V IO. Three power modes are provided in SPC1169 as below.

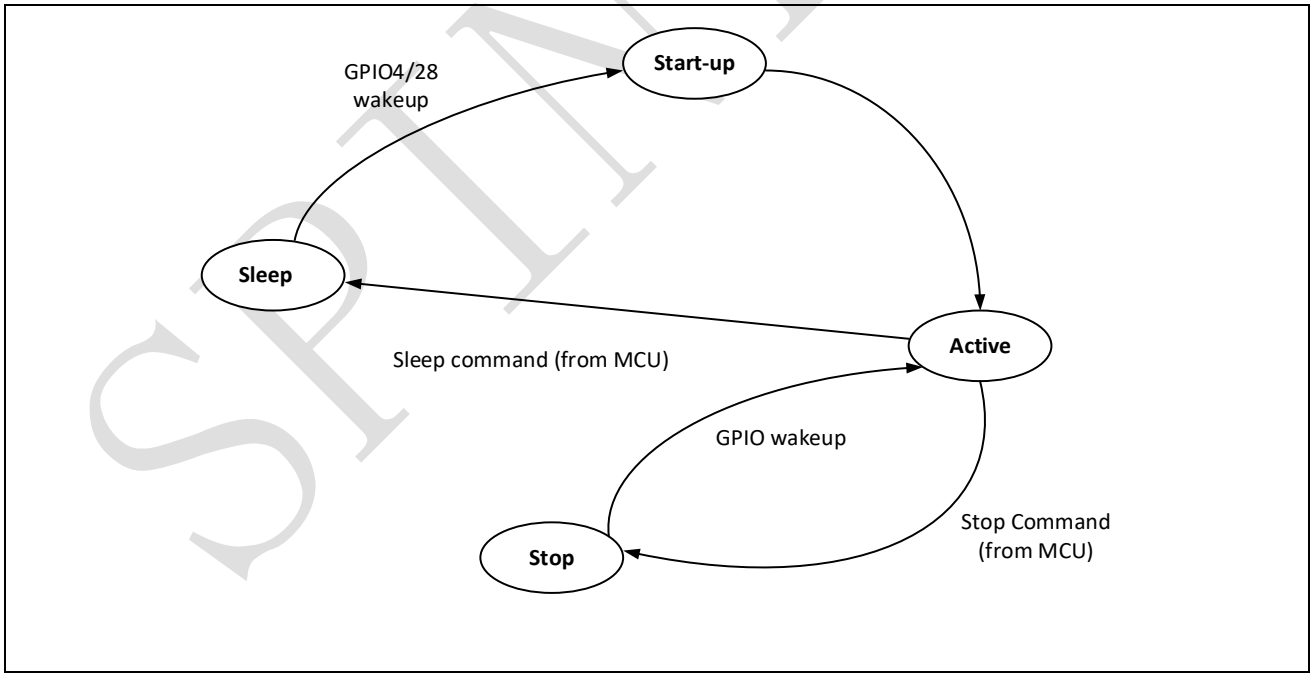
- Active mode
  VCAP12 rail is supplied by on-chip LDO with full current driving capability. All clocks are enabled per user's setup in register control bits.
- Stop mode
  All clocks are stopped except for the 100kHz clock for power mode state machine. VCAP12 rail is supplied by low-power LDO with limited current driving capability. It can be configured to be below 1.2 V to further reduce the static current. All registers and memories retain the content. The system can be waken-up by any GPIO per user's setup with programmable input levels. The CPU will continue to run the instructions when it entered stop mode.
- Sleep mode
  VCAP12 is totally shutdown. It can be waken-up by GPIO and the whole system will go through a cold boot-up.

Figure 2-1: Power management module



The Power Management Unit (PMU) is responsible for supplying all the voltages required for the embedded MCU (VCAP12). The PMU has a clearly defined state machine to control the transition of the power mode, as shown in Figure 2-2.

Figure 2-2: Power mode conversion



2.12 Boot mode

The boot code is located in on-chip ROM memory. After reset, the ARM processor starts code execution from the ROM. The boot pin and TRSTn pin are used to select one of the two boot options:

- Boot from embedded Flash (boot pin = 0, TRSTn pin = X): the boot loader jumps to the embedded Flash and runs from the address at 0x1000 0000

- ISP mode (boot pin = 1, TRSTn pin = 0): the boot loader reprograms the embedded Flash by using UART or LIN interface. During the process, if using UART interface, the GPIO10 is configured as UART0_TXD and the GPIO11 is configured as UART0_RXD.

Note: 1. The TRSTn pin is recommended to set as low.
2. When TRSTn is high, GPIO15 ~ GPIO18 worked as debug interface pins.

2.13 General-purpose IOs (GPIOs)

The SPC1169 can be configured to support as many as 37 multi-purpose GPIO pins. Each GPIO pin can be configured by software as input, as output or as peripheral alternate function. It features:

- Each GPIO pin has configurable internal pull-up and pull-down resistors
- Each GPIO pin has a programmable digital input deglitch filter
- Pure 3.3V I/O capability multiplexed with ADC input channel for GPIO0~GPIO4/GPIO28~GPIO31/ GPIO36~GPIO40
- Full 5V I/O capability for GPIO5 ~ GPIO24/GPIO32 ~ GPIO35 if 5V power is applied to DVDD5 pin

Note: The boot pin can be configured as GPIO5 with limitations. Please make sure the pin level is low when the device is resetting, or the device will enter ISP mode.

2.14 Timers and watchdogs

The SPC1169 device includes three general-purpose timers, two watchdog timers and a SysTick timer.

General-purpose timers

The SPC1169 includes three identical 32-bit general-purpose timers. Each general-purpose timer consists of a 32-bit auto-reload down-counter. An interrupt would be generated when the counter reaches zero if it is enabled. When the counter reaches zero, the timer can also generate an ADCSOC event or a PWMSYNC event if they are enabled. The clock of general-purpose timer can be selected from internal RC oscillators, external oscillator or PLL clock. Besides, each general-purpose timer can also be configured to use external pin as enable control, event for the counter, or event to capture current counter value.

Watchdogs

The SPC1169 implements two identical watchdogs. Each watchdog is based on a 32-bit down-counter, which can be clocked from internal RC oscillators, external oscillator or PLL clock. When the counter reaches the given time-out value, an interrupt or a reset can be generated. The watchdog counter can be frozen or free-running in debug mode.

SysTick Timer

This timer is dedicated for OS, but could also be used as a standard down-counter. It features:

- A 24-bit down-counter
- Auto-reload capability
- Mask-able system interrupt generation when the counter reaches 0

2.15 UART

The SPC1169 has two UART modules. They features:

- Ability to add or delete standard asynchronous communication bits (start, stop and parity) in the serial data
- 5 – 8 data bits
- Even, odd or no parity detection
- One, one-and-a-half, or two stop bits generation
- Baud-rate generation up to 6.25 Mbps
- 64-byte transmit FIFO
- 64-byte receive FIFO
- Auto baud-rate detection

Specific hardware is also implemented to enable LIN features:

- Compatibility with LIN 2.2 protocols
- Configurable baud rate up to 20 kbps
- Identification masks for message filtering
- Hardware processing on break field, sync byte field, protected ID field, data field and checksum field
- Response length can be defined by bit 5 and bit 4 of protected ID field, or by register control
- Programmable classic checksum mode or enhanced checksum mode

2.16 I2C

The I^2C bus interface complies with the common I^2C protocol. It features:

- Four speeds: Standard mode (100 Kb/s), Fast mode (400 Kb/s), Fast mode plus (1 Mb/s) and High-Speed mode (3.4 Mb/s)
- Clock synchronization
- Master or slave I2C operation
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- 16 x 32-bit deep transmit and receive buffers, respectively

2.17 SPI

SPC1169 includes two SPI modules, which allow half/full-duplex, synchronous, serial communication with external devices. They features:

- Full-duplex synchronous transfers
- Master or slave operation
- 1 to 32-bit transfer frame format selection
- Local clock divider for flexible communication speed control, with up to 50 Mbps capability
- MSB-first data order
- Programmable clock polarity and phase
- 16 x 32-bit deep transmit and receive FIFOs, respectively

2.18 CAN

The SPC1169 has implemented one CAN module. The CAN module performs CAN protocol communication according to ISO 11898-1. A CAN transceiver chip is required for the connection to the physical layer (CAN bus). The CAN module features:

- Compatible with Bosch CAN2.0B and Bosch CANFD 1.0 protocol
- Compatible with the ISO11898-1:2015 (CAN 2.0 and CANFD) protocol specification
- 64 mailboxes
- Individual identifier mask for each mailbox
- Support CAN error recording
- Timestamp counter

Note: The CAN module of SPC1169 does not support wake-up function, users need to select a CAN PHY that supports wake-up function and connect the CAN PHY wake-up signal to the GPIO pin of SPC1169 to realize the CAN wake-up function.

2.19 ADC

One 13-bit analog-to-digital convert is embedded into SPC1169 and has up to 14 external channels. The temperature sensor, internal powers and PGA outputs can be selected as ADC input channels. These inputs are multiplexed. The ADC core has built-in sample-and-hold (S/H) with two input channels, which is suitable for differential sampling. The start of sample and conversion can be triggered by the software, the internally connected hardware event signals from the general-purpose timers and the PWM outputs, or from the external pin input.

The 13-bit ADC features

- 200 ns minimum conversion time and independent configurable sampling time
- Differential sampling
- Full range analog input: 0 V to 3.65 V
- Reference voltage can be selected from internal or external
- Input open and short detection for safety

Another 13-bit ADC (Monitoring ADC) is provided to routinely check critical voltages below per user's request for system safety concern. An interrupt can be generated if the monitoring item is out of the pre-defined range.

Please see Table 5-16 for 13-bit ADC characteristics and Table 5-17 for Monitoring ADC characteristics.

2.20 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. It is internally connected to the ADC input channel, which is used to convert the sensor output voltage into a digital value.

2.21 PGAs

SPC1169 includes a differential programmable gain amplifier (DPGA) with two dedicated pins. It features:

- Programmable gains: 2, 4, 8, 16, 24, 32, 48 and 64
- Differential input voltage: ±2.7V/PGA_Gain
- Wide common mode input range: -0.5V ~ 2V
- Settling time: 250 ns to 1.4 us

A single-ended PGA (SPGA) is also implemented in SPC1169. The four external ADC input channels (ANA_IN0~ANA_IN3), the temperature sensor output, and internal 1.2V power can be selected as the SPGA input. It features:

- Programmable gains: 1, 2, 4, 8, 16, 32, 48 and 64
- Settling time: 300 ns to 2 us

Both the outputs from the differential PGA (DPGA) and the single-ended PGA (SPGA) can be selected as the 13-bit ADC input. Please see Table 5-19 for DPGA characteristics and Table 5-20 for SPGA characteristics.

2.22 Analog comparators

The SPC1169 has two high-speed comparators, which are used with two internal 10-bit DAC as reference for monitoring PGA inputs or outputs to check whether the voltage is too high or too low. The comparator output is routed to the PWM Trip-Zone modules.

- 50 ns typical response
- Programmable hysteresis
- Output with digital deglitch filter

Please see Table 5-21 and Table 5-23 for analog comparator and DAC characteristics.

2.23 Phase comparators

SPC1169 has 3 high speed rail-to-rail phase comparators, which can compare three phases voltage (PHU/PHV/PHW) to the common mode voltage (PHC). Phase comparator has 8-to-1 input MUX, it can also use as normal comparator to compare analog ADC input to reference voltage (ADC input or DAC output).

Based on the intrinsic characteristic of motor operation, hardware post-processing is implemented to the comparator output as below, so as to simplify user's software.

- Blanking with programmable window size
- Filtering with programmable window size
- Finite state machine (FSM) to ignore the systematic false alarm due to the large interferences via motor toggling. The FSM can be reset to initial state per user's software. The first zero-crossing event after the FSM reset is ignored.

2.24 DAC and DAC buffer

The SPC1169 has three 10-bit DACs that generate a voltage from 0 to VDDA. Among them, DAC0 and DAC1 are used to simulate the comparator to judge the reference voltage that is too high or too low, and DAC2 can be used as the reference voltage for the phase comparator. The DAC usually generates static voltage as the threshold of the comparator and does not guarantee the performance of dynamically changing the code value to generate the waveform.

The SPC1169 has one DAC buffer, it can select DAC0 or DAC1 as its input, and send output through ANA_IN2 pin.

2.25 D2S buffer

The SPC1169 integrates one D2S (differential to single-ended) buffer, which can convert DPGA's differential output voltage to single-ended output voltage and sent it to ANA_IN4 pin. Through external RC filter (typically, R = 1kΩ, C = 1uF), the single-ended output voltage can be sent back to ANA_INx (x = 0 ~ 3) pin and measured by 13-bit ADC. D2S buffer gain is fixed at 0.5.

2.26 PWMs

The SPC1169 integrates four PWM modules and supports eight PWM channels. Without much involvement of processor core, the PWMs can generate complex pulse width waveforms.

Each PWM module supports the following features:

- Dedicated 16-bit time-base counter with period and frequency control
- Each PWM module can generate two outputs with single-edge operation, dual-edge symmetric operation or dual-edge asymmetric operation
- All events can trigger both CPU interrupts and ADC start of conversion
- Programmable phase-control support for lag or lead operation relative to other PWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both cycle-by-cycle trip and one-shot trip on fault conditions
- A trip condition can force either high, low, or high-impedance state logic levels at PWM outputs
- Comparator module outputs and trip zone inputs can generate events, filtered events, or trip conditions

2.27 ECAP

The enhanced capture (ECAP) module is essential in systems where accurate timing of external events is important. The SPC1169 has implemented an ECAP module with following features:

- Flexible input capture pin: each GPIO can be configured as capture pin
- 32-bit time base counter
- 4 x 32-bit time-stamp capture registers
- 4-stage sequencer that is synchronized to external events
- Independent edge polarity (rising/falling edge) selection for all 4 events
- Interrupt capabilities on any of the 4 capture events

2.28 Cyclic redundancy check (CRC)

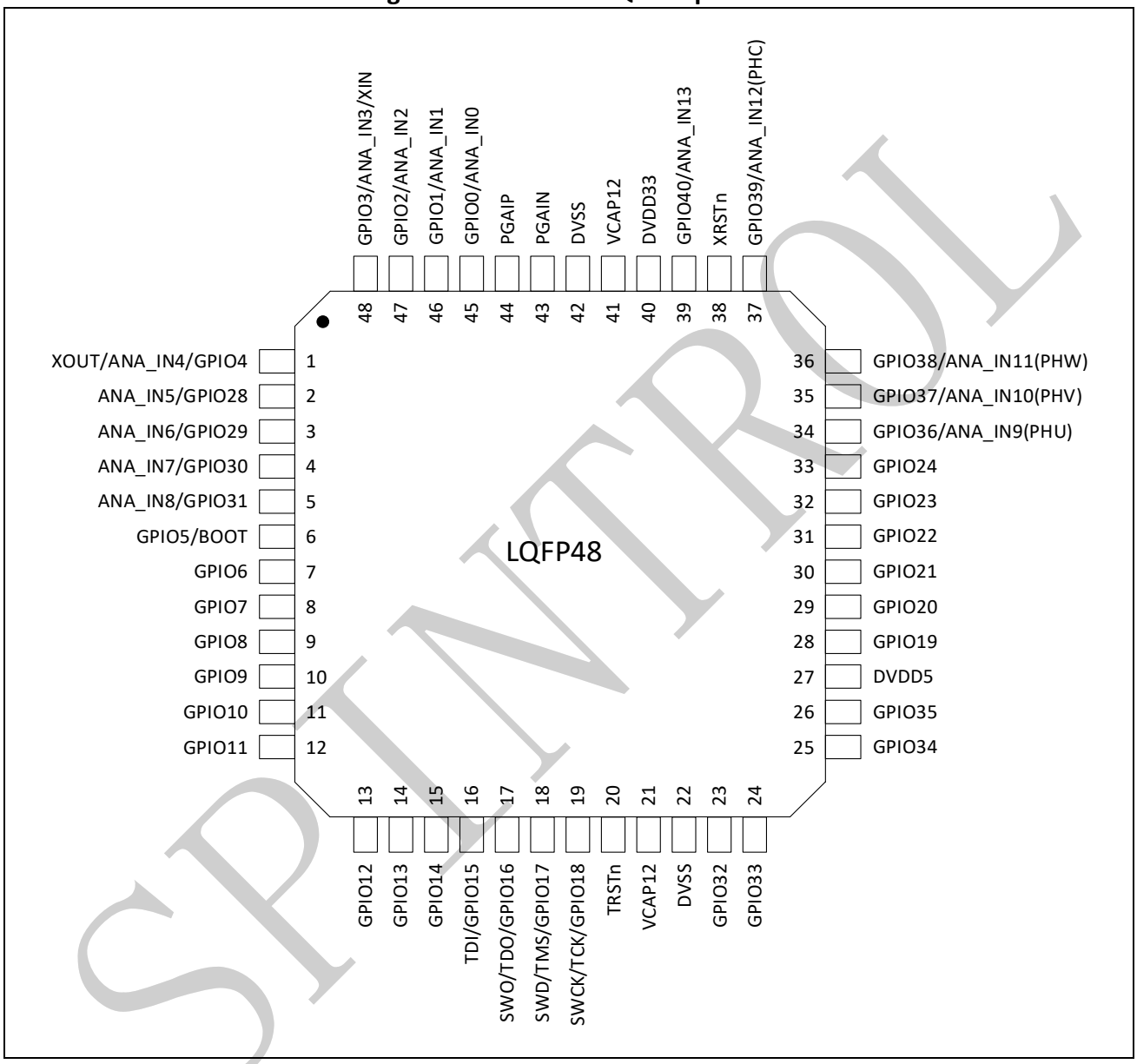
The SPC1169 has a hardware CRC calculation unit. The CRC module is used to verify data transmission or storage integrity. It features:

- 32-bit parallel bit stream input, and up to 32-bit CRC output
- Supports up to 232 byte length for CRC calculation
- Eight CRC standard polynomials supported

3 Pinouts and pin description

3.1 LQFP48

Figure 3-1: SPC1169 LQFP48 pinout



[1] The above figure shows the package top view.

[2] **Note: when TRSTn is HIGH, GPIO15 ~ GPIO18 pins work as Debug interface.**

Table 3-1: SPC1169 LQFP48 pin definitions

Pin	Type	Signal	Sub-Type[1]	Description
1	3.3V I/O	GPIO4	I/O	General-purpose input/output 4
		ANA_IN4	AI	Analog input channel 4
		XOUT	O	External oscillator output
		COMP_MON1	O	Comparator output monitor 1
2	3.3V I/O	GPIO28	I/O	General-purpose input/output 28
		ANA_IN5	AI	Analog input channel 5
		SPI1_SCLK	I/O	SPI1 clock input/output
		PWMSOCAO	O	PWMSOCA output
3	3.3V I/O	GPIO29	I/O	General-purpose input/output 29
		ANA_IN6	AI	Analog input channel 6
		SPI1_SFRM	I/O	SPI1 frame signal input/output
		PWMSOCBO	O	PWMSOCB output
4	3.3V I/O	GPIO30	I/O	General-purpose input/output 30
		ANA_IN7	AI	Analog input channel 7
		SPI1_MOSI	I/O	SPI1 master output, slave input
		PWMSOCCO	O	PWMSOCC output
5	3.3V I/O	GPIO31	I/O	General-purpose input/output 31
		ANA_IN8	AI	Analog input channel 8
		SPI1_MISO	I/O	SPI1 master input, slave output
		PWMSYNCO	O	PWMSYNC output
6	5V I/O	BOOT(GPIO5)	I/O	Boot pin (General-purpose input/output 5)
		PWMSOCO	O	PWMSOC output for monitoring It is the logic OR of PWMSOCAO, PWMSOCBO and PWMSOCCO.
		ECAP_APWMO	O	APWM mode output of the ECAP
7	5V I/O	GPIO6	I/O	General-purpose input/output 6
		SPI0_SCLK	I/O	SPI0 clock input/output
		UART1_TXD	O	UART1 transmitted data
		COMP_MON2	O	Comparator output monitor 2
8	5V I/O	GPIO7	I/O	General-purpose input/output 7
		SPI0_SFRM	I/O	SPI0 frame signal input/output
		UART1_RXD	I	UART1 received data
		COMP_MON3	O	Comparator output monitor 3
9	5V I/O	GPIO8	I/O	General-purpose input/output 8
		SPI0_MOSI	I/O	SPI0 master output, slave input
		CAN_TXD	O	SPI0 master input, slave output
		COMP_MON4	O	Comparator output monitor 4
10	5V I/O	GPIO9	I/O	General-purpose input/output 9
		SPI0_MISO	I/O	SPI0 master input, slave output
		CAN_RXD	I	SPI0 master output, slave input
		COMP_MON5	O	Comparator output monitor 5
11	5V I/O	GPIO10	I/O	General-purpose input/output 10

Pin	Type	Signal	Sub-Type[1]	Description
		UART0_TXD	O	UART0 transmitted data
		PWM0A	O	PWM0 output A
		I2C_SCL	I/O	I2C clock
12	5V I/O	GPIO11	I/O	General-purpose input/output 11
		UART0_RXD	I	UART0 received data
		PWM0B	O	PWM0 output B
		I2C_SDA	I/O	I2C data
13	5V I/O	GPIO12	I/O	General-purpose input/output 12
		SPI1_SCLK	I/O	SPI1 clock input/output
		PWM1A	O	PWM1 output A
		PWM3A	O	PWM3 output A
14	5V I/O	GPIO13	I/O	General-purpose input/output 13
		SPI1_SFRM	I/O	SPI1 frame signal input/output
		PWM1B	O	PWM1 output B
		PWM3B	O	PWM3 output B
15	5V I/O	GPIO14	I/O	General-purpose input/output 14
		SPI1_MOSI	I/O	SPI1 master output, slave input
		PWM2A	O	PWM2 output A
		I2C_SCL	I/O	I2C clock
16	5V I/O	GPIO15	I/O	General-purpose input/output 15
		SPI1_MISO	I/O	SPI1 master input, slave output
		PWM2B	O	PWM2 output B
		I2C_SDA	I/O	I2C data
		TDI	I	JTAG data input
		Note: when TRSTn is HIGH and JTAG debug mode is selected, this pin always works as TDI and can't be configured as other functions.		
17	5V I/O	GPIO16	I/O	General-purpose input/output 16
		UART1_TXD	O	UART1 transmitted data
		CAN_TXD	O	CAN transmitted data
		SPI1_SFRM	I/O	SPI1 frame signal input/output
		TDO/SWO	O	JTAG data output or Asynchronous TRACE output
		Note: when TRSTn is HIGH and JTAG debug mode is selected, this pin always works as TDO/SWO and can't be configured as other functions; when SWD debug mode is selected and Debug Trace is enabled, this pin always works as SWO and can't be configured as other functions.		
18	5V I/O	GPIO17	I/O	General-purpose input/output 17
		UART1_RXD	I	UART1 received data
		CAN_RXD	I	CAN received data
		SPI1_SCLK	I/O	SPI1 clock input/output
		TMS/SWD	I/O	JTAG mode select or SWD data
		Note: when TRSTn is HIGH, this pin always works as TMS/SWD and can't be configured as other functions.		

Pin	Type	Signal	Sub-Type[1]	Description
19	5V I/O	GPIO18	I/O	General-purpose input/output 18
		PWMSOCO	O	PWMSOC output for monitoring It is the logic OR of PWMSOCAO, PWMSOCBO and PWMSOCCO
		PWMSYNCO	O	PWMSYNC output
		ECAP_APWMO	O	APWM mode output of the ECAP
		TCK/SWCK	I	JTAG clock or SWD clock
		Note: when TRSTn is HIGH, this pin always works as TCK/SWCK and can't be configured as other functions.		
20	5V I/O	TRSTn	I	JTAG reset pin, reset the JTAG when low
21	1.2V Power	VCAP12	P	1.2 V power **Add 0.1uF bypass ceramic cap to DVSS**
22	Ground	DVSS	G	Digital ground
23	5V I/O	GPIO32	I/O	General-purpose input/output 32
		UART1_TXD	O	UART1 transmitted data
		I2C_SCL	I/O	I2C clock
		COMP_MON6	O	Comparator output monitor 6
24	5V I/O	GPIO33	I/O	General-purpose input/output 33
		UART1_RXD	I	UART1 received data
		I2C_SDA	I/O	I2C data
		COMP_MON7	O	Comparator output monitor 7
25	5V I/O	GPIO34	I/O	General-purpose input/output 34
		CAN_TXD	O	CAN transmitted data
		I2C_SCL	I/O	I2C clock
26	5V I/O	GPIO35	I/O	General-purpose input/output 35
		CAN_RXD	I	CAN received data
		I2C_SDA	I/O	I2C data
27	5V Power	DVDD5	P	5.5 V digital power DVDD5=5.0V: GPIO5 ~ GPIO24 are 5V I/O DVDD5=3.3V: GPIO5 ~ GPIO24 are 3.3V I/O **Add 4.7uF and 0.1uF bypass ceramic cap to DVSS**
28	5V I/O	GPIO19	I/O	General-purpose input/output 19
		PWM2B	O	PWM2 output B
		PWM0A	O	PWM0 output A
		ECAP_APWMO	O	APWM mode output of the ECAP
29	5V I/O	GPIO20	I/O	General-purpose input/output 20
		PWM2A	O	PWM2 output A
		PWM1A	O	PWM1 output A
		ECAP_APWMO	O	APWM mode output of the ECAP
30	5V I/O	GPIO21	I/O	General-purpose input/output 21
		PWM1B	O	PWM1 output B
		PWM2A	O	PWM2 output A

Pin	Type	Signal	Sub-Type[1]	Description
		ECAP_APWMO	O	APWM mode output of the ECAP
31	5V I/O	GPIO22	I/O	General-purpose input/output 22
		PWM1A	O	PWM1 output A
		PWM0B	O	PWM0 output B
		ECAP_APWMO	O	APWM mode output of the ECAP
32	5V I/O	GPIO23	I/O	General-purpose input/output 23
		PWM0B	O	PWM0 output B
		PWM1B	O	PWM1 output B
		ECAP_APWMO	O	APWM mode output of the ECAP
33	5V I/O	GPIO24	I/O	General-purpose input/output 24
		PWM0A	O	PWM0 output A
		PWM2B	O	PWM2 output B
		ECAP_APWMO	O	APWM mode output of the ECAP
34	3.3V I/O	GPIO36	I/O	General-purpose input/output 36
		ANA_IN9(PHU)	AI	ADC channel 9 input (U-phase input channel for phase comparison)
		SPI1_SCLK	I/O	SPI1 clock input/output
		UART1_TXD	O	UART1 transmitted data
35	3.3V I/O	GPIO37	I/O	General-purpose input/output 37
		ANA_IN10(PHV)	AI	ADC channel 10 input (V-phase input channel for phase comparison)
		SPI1_SFRM	I/O	SPI1 frame signal input/output
		UART1_RXD	I	UART1 received data
36	3.3V I/O	GPIO38	I/O	General-purpose input/output 38
		ANA_IN11(PHW)	AI	ADC channel 11 input (W-phase input channel for phase comparison)
		SPI1_MOSI	I/O	SPI1 master output, slave input
		CAN_TXD	O	CAN transmitted data
37	3.3V I/O	GPIO39	I/O	General-purpose input/output 39
		ANA_IN12(PHC)	AI	ADC channel 12 input (Common reference input for phase comparison)
		SPI1_MISO	I/O	SPI1 master input, slave output
		CAN_RXD	I	CAN received data
38	3.3V I/O	XRSTn	I	Device reset pin, reset the device when low
39	3.3V I/O	GPIO40	I/O	General-purpose input/output 40
		ANA_IN13	AI	ADC channel 13 input
40	3.3V Power	DVDD33	P	3.3 V digital power **Add 4.7uF and 0.1uF bypass ceramic cap to DVSS**
41	1.2V Power	VCAP12	P	1.2 V power **Add 4.7uF and 0.1uF bypass ceramic cap to DVSS**
42	Ground	DVSS	G	Digital ground

Pin	Type	Signal	Sub-Type[1]	Description
43	-2V ~ 3.3V input	PGAIN	AI	Differential PGA negative input
44	-2V ~ 3.3V input	PGAIP	AI	Differential PGA positive input
45	3.3V I/O	GPIO0	I/O	General-purpose input/output 0
		ANA_IN0	AI	Analog input channel 0
		PWMSOCAO	O	PWMSOCA output
		PWMSOCCO	O	PWMSOCC output
46	3.3V I/O	GPIO1	I/O	General-purpose input/output 1
		ANA_IN1	AI	Analog input channel 1
		PWMSOCB	O	PWMSOCB output
		ECAP_APWMO	O	APWM mode output of the ECAP
47	3.3V I/O	GPIO2	I/O	General-purpose input/output 2
		ANA_IN2	AI	Analog input channel 2
		DCLK	O	Clock output from CLKDET module for monitoring
48	3.3V I/O	GPIO3	I/O	General-purpose input/output 3
		ANA_IN3	AI	Analog input channel 3
		XIN	AI	External oscillator input
		COMP_MON0	O	Comparator output monitor 0

[1] I = digital input, O = digital output, AI = analog input, AO = analog out, P = power supply, G = ground.

3.2 GPIO pin function and state after reset

Table 3-2: GPIO pin function and state after reset

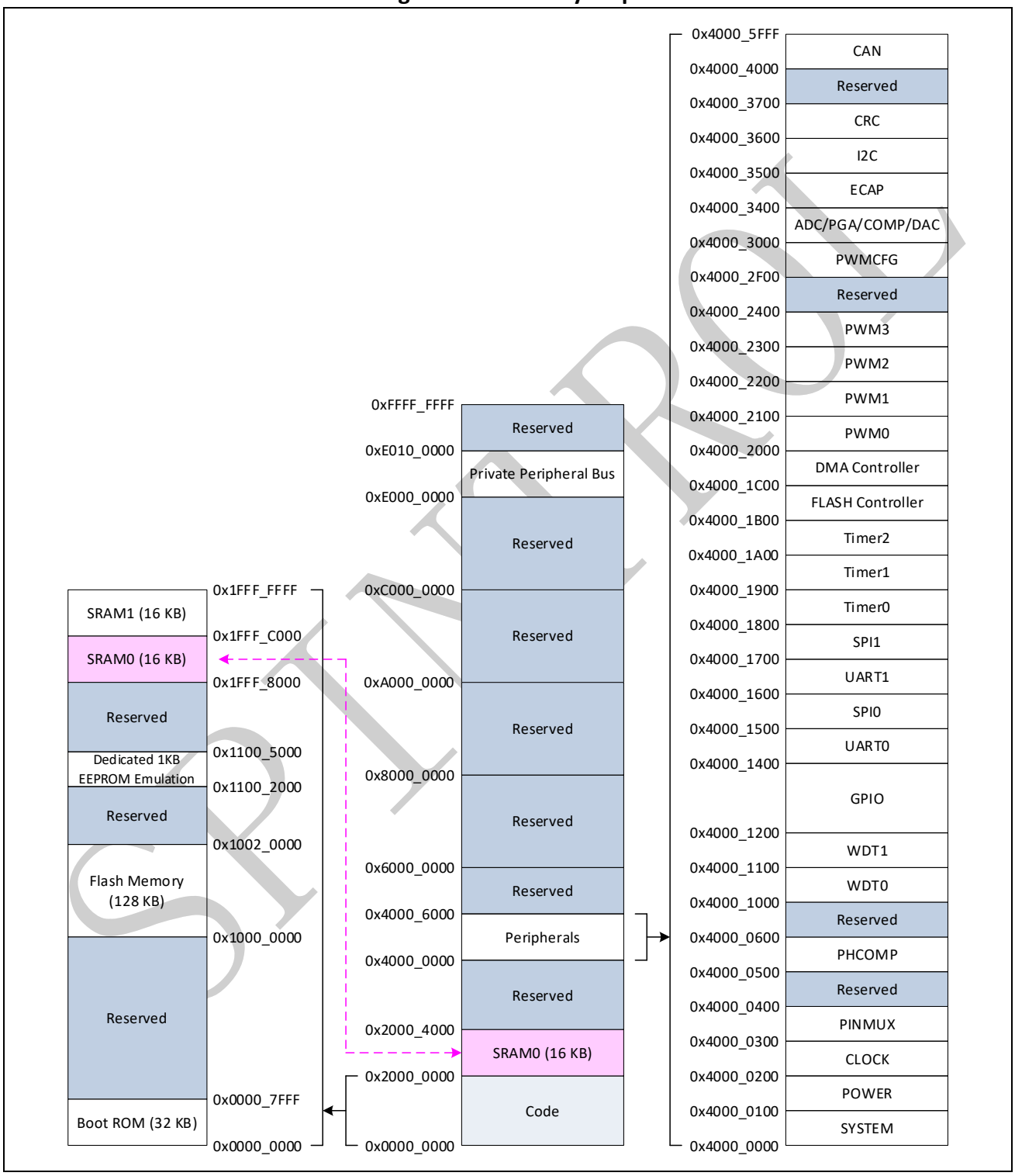
Pin Name	Default Function	Default State
GPIO0	ANA_IN0	浮空
GPIO1	ANA_IN1	浮空
GPIO2	ANA_IN2	浮空
GPIO3	ANA_IN3	浮空
GPIO4	ANA_IN4	浮空
GPIO5	GPIO5/BOOT	下拉
GPIO6	GPIO6	上拉
GPIO7	GPIO7	上拉
GPIO8	GPIO8	上拉
GPIO9	GPIO9	上拉
GPIO10	GPIO10	上拉
GPIO11	GPIO11	上拉
GPIO12	GPIO12	浮空
GPIO13	GPIO13	浮空
GPIO14	GPIO14	上拉
GPIO15	GPIO15	上拉
GPIO16	GPIO16	上拉

Pin Name	Default Function	Default State
GPIO17	GPIO17	上拉
GPIO18	GPIO18	下拉
GPIO19	GPIO19	浮空
GPIO20	GPIO20	浮空
GPIO21	GPIO21	浮空
GPIO22	GPIO22	浮空
GPIO23	GPIO23	浮空
GPIO24	GPIO24	浮空
~~GPIO25~~	~~GPIO25~~	上拉
~~GPIO26~~	~~GPIO26~~	上拉
~~GPIO27~~	~~GPIO27~~	下拉
GPIO28	ANA_IN5	浮空
GPIO29	ANA_IN6	浮空
GPIO30	ANA_IN7	浮空
GPIO31	ANA_IN8	浮空
GPIO32	GPIO32	上拉
GPIO33	GPIO33	上拉
GPIO34	GPIO34	上拉
GPIO35	GPIO35	上拉
GPIO36	ANA_IN9	浮空
GPIO37	ANA_IN10	浮空
GPIO38	ANA_IN11	浮空
GPIO39	ANA_IN12	浮空
GPIO40	ANA_IN13	浮空

4 Memory mapping

The memory map of SPC1169 is shown in Figure 4-1.

Figure 4-1: Memory map



5 Electrical characteristics

5.1 Absolute maximum ratings

Table 5-1: Absolute maximum ratings[1][2]

Symbol	Parameter	Min	Max	Unit
V_{DVDD5}	5V digital supply voltage, with respect to VSS	-0.3	6.5	V
V_{DVDD33}	3.3V digital supply voltage, with respect to VSS	-0.3	4.6	V
V_{IN_5V}	5V IO input voltage	-0.3	V_{DVDD5} + 0.3	V
V_{IN_3V}	3.3V IO input voltage	-0.3	V_{DVDD33} + 0.3	V
I_{IC}	Input clamp current	-20	+20	mA
I_{OC}	Output clamp current	-20	+20	mA
T_J	Junction temperature[3]	-40	+150	°C
T_{stg}	Storage temperature[3]	-65	+150	°C

[1] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these is not implied.

[2] All voltage values are with respect to VSS, unless otherwise noted.

[3] Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life.

5.2 Recommended operating conditions

Table 5-2: Recommended operating conditions

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DVDD5}	5V supply voltage	–	2.97	5.0	5.5	V
V_{DVDD33}	3.3V supply voltage	–	2.97	3.3	3.63	V
V_{DVSS}	Supply ground	–	–	0	–	V
V_{IH_5V}	5V high-level input voltage	V_{DVDD5} = 5 V	–	3.5	V_{DVDD5}+0.3	V
V_{IL_5V}	5V low-level input voltage	V_{DVDD5} = 5 V	V_{DVSS}-0.3	1.5	–	V
I_{OH_5V}	5V high-level output source current when VOH = 4.0V, VDD5=4.5V	STRENGTH=0 STRENGTH=1	–	–	0.4 7.3	mA
I_{OL_5V}	5V low-level output sink current when VOL = 0.4V, VDD5=4.5V	STRENGTH=0 STRENGTH=1	–	–	1.74 26.1	mA
V_{IH_3V}	3.3V high-level input voltage	V_{DD33} = 3.3 V	2.0	–	V_{DVDD33}+0.3	V
V_{IL_3V}	3.3V low-level input voltage	V_{DD33} = 3.3 V	V_{DVSS}-0.3	–	0.8	V
I_{OH_3V}	3.3V high-level output source current when VOH = VOH(MIN)	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
I_{OL_3V}	3.3V low-level output sink current when VOL = VOL(MAX)	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
T_J	Junction temperature	–	-40	–	+150	°C

5.3 Electrical characteristics

Table 5-3: 5V IO Electrical characteristics (V_{DVDD5}=5V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = $I_{OH\ MAX}$	V_{DVDD5} - 1	–	–	V
V_{OL}	Low-level output voltage	I_{OL} = $I_{OL\ MAX}$	–	–	1	V
V_{IH}	High-level input voltage	–	TBD	3.5	V_{DVDD5} + 0.3	V
V_{IL}	Low-level input voltage	–	V_{SS} - 0.3	1.5	TBD	V
I_{OH}	High-level output source current when V_{OH} = $V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1	–	–	0.4 7.3	mA
I_{OL}	Low-level output sink current when V_{OL} = $V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1	–	–	1.74 26.1	mA
I_{IL}	Low-level input current (Pin with pull-down enabled)	V_{IH} = 0 V	–	–	10	uA
I_{IH}	High-level input current (Pin with pull-down enabled)	V_{IH} = V_{DVDD5}	–	–	10	uA
R_{PU}	Input pull-up resistor	V_{IO} = 0 V	–	50	–	kΩ
R_{PD}	Input pull-down resistor	V_{IO} = V_{DVDD5}	–	50	–	kΩ

Table 5-4: 5V IO Electrical characteristics (V_{DVDD5}=3.3V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = $I_{OH\ MAX}$	V_{DVDD5} - 1	–	–	V
V_{OL}	Low-level output voltage	I_{OL} = $I_{OL\ MAX}$	–	–	1	V
V_{IH}	High-level input voltage	–	TBD	2.4	V_{DVDD5} + 0.3	V
V_{IL}	Low-level input voltage	–	V_{SS} - 0.3	0.8	TBD	V
I_{OH}	High-level output source current when V_{OH} = $V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1	–	–	0.23 4.1	mA
I_{OL}	Low-level output sink current when V_{OL} = $V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1	–	–	0.97 14.5	mA
I_{IL}	Low-level input current (Pin with pull-down enabled)	V_{IH} = 0 V	–	–	10	uA
I_{IH}	High-level input current (Pin with pull-down enabled)	V_{IH} = V_{DVDD5}	–	–	10	uA
R_{PU}	Input pull-up resistor	V_{IO} = 0 V	–	50	–	kΩ
R_{PD}	Input pull-down resistor	V_{IO} = V_{DVDD5}	–	50	–	kΩ

Table 5-5: 3.3V IO Electrical characteristics (V_{DVDD33}=3.3V)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	I_{OH} = $I_{OH\ MAX}$	V_{DVDD33}-0.66	–	–	V
V_{OL}	Low-level output voltage	I_{OL} = $I_{OL\ MAX}$	–	–	0.66	V
V_{IH}	High-level input voltage	–	2.0	–	V_{DVDD33} + 0.3	V
V_{IL}	Low-level input voltage	–	V_{DVSS}-0.3	–	0.8	V
I_{OH}	High-level output source current when V_{OH} = $V_{OH(MIN)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
I_{OL}	Low-level output sink current when V_{OL} = $V_{OL(MAX)}$	STRENGTH=0 STRENGTH=1 STRENGTH=2 STRENGTH=3	–	–	5 10 15 20	mA
I_{IL}	Low-level input current (Pin with pull-down enabled)	V_{DVDD33} = 3.3V V_{IH} = 0 V	–	–	10	uA
I_{IH}	High-level input current (Pin with pull-down enabled)	V_{DVDD33} = 3.3V V_{IH} = V_{DVD33}	–	–	10	uA
R_{PU}	Input pull-up resistor	V_{IO} = 0 V	–	41	–	kΩ
R_{PD}	Input pull-down resistor	V_{IO} = V_{DVDD33}	–	42	–	kΩ

5.4 Power mode transition time

Table 5-6: Power mode transition time

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{stop,entry}$	Stop mode entry time	–	–	25	–	us
$t_{stop,exit}$	Stop mode exit time (to user's code)	–	–	1	–	ms
$t_{sleep,entry}$	Sleep mode entry time	–	–	25	–	us
$t_{sleep,exit}$[1]	Sleep mode exit time (to user's code)	–	–	7.4	–	ms

[1] It contain ~5.63ms for the RAM self-test.

5.5 Power consumption summary

Typical current consumption

In operational mode, the SPC1169 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are enabled;
- All peripheral clocks are as fast as HCLK (frequency division is 1), except SPI (Max 50 MHz) and DGCLK (Max 50 MHz);
- All clock modules are enabled;
- Select PLL clock as system clock source.

In idle mode, the SPC1169 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are clocked off or disabled;
- Clock modules (PLL, RCO0 and XO) are disabled;
- Select RCO1 as system clock source.

In stop mode, the SPC1169 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are clocked off or disabled;
- Clock modules (PLL, RCO0, RCO1 and XO) are disabled;
- 1.2V LDO still exist and enter to low power mode.

In sleep mode, the SPC1169 is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals (including analog module) are clocked off or disabled;
- Clock modules (PLL, RCO0, RCO1 and XO) are disabled;
- 1.2V LDO is shut down to 0V.

The typical current consumption of SPC1169 measured from VDD is shown in Table 5-7 and Table 5-8. The operational current consumption over various HCLK frequency is shown in Figure 5-1.

Table 5-7: SPC1169 typical current consumption (Run in FLASH)

Mode	Condition		Typ	Unit
	f_{HCLK}	f_{PLL}		
Operational	100 MHz	100 MHz	25.489	mA
	75 MHz	75 MHz	22.676	mA
	50 MHz	50 MHz	19.645	mA
	32 MHz	32 MHz	17.565	mA
	25 MHz	25 MHz	16.328	mA
Idle	–	–	6.261	mA
Stop[2]	–	–	134.431	uA
Sleep[2]	–	–	1.011	uA

[1] Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V.

[2] BOOT pin is connected to GND.

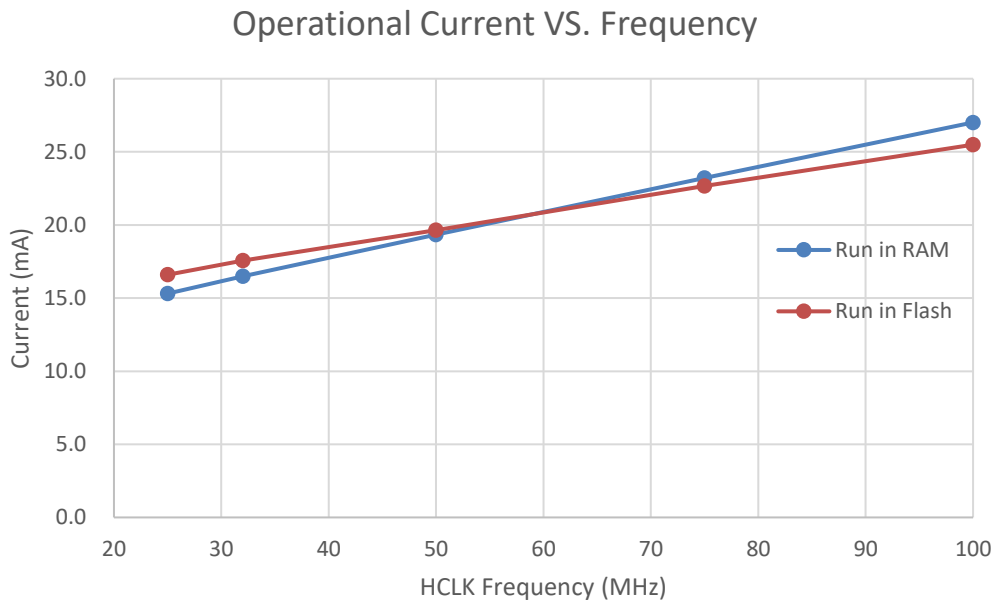
Table 5-8: SPC1169 typical current consumption (Run in RAM)

Mode	Condition		Typ	Unit
	f_{HCLK}	f_{PLL}		
Operational	100 MHz	100 MHz	27.009	mA
	75 MHz	75 MHz	23.213	mA
	50 MHz	50 MHz	19.337	mA
	32 MHz	32 MHz	16.492	mA
	25 MHz	25 MHz	15.307	mA
Idle	–	–	5.456	mA
Stop[2]	–	–	125.781	uA

[1] Typical values are measured at TA = 25 °C, VDD = 3.3 V.

[2] BOOT pin is connected to GND.

Figure 5-1: Typical operational current versus frequency



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 5-9. The MCU is placed under the following conditions:

- All I/O pins are in input mode and left unconnected;
- All peripherals(including analog module, RCO0 and XO) are disabled unless otherwise mentioned;
- The given value is calculated by measuring the current consumption
  - With all peripherals clocked disabled
  - With only one peripheral enabled

Table 5-9: Peripheral current consumption

Peripherals[1]	Condition	Typ[2]	Unit
BOD	Select RCO0 as system clock source; All other peripherals are in default settings	90	uA
ADC[3]	Select PLL clock as system clock source; All peripheral clocks are as fast as HCLK; f_{HCLK} = 100 MHz, f_{PLL} = 100 MHz	8330	uA
Monitor ADC[3]		2870	uA
T-sensor		150	uA
DPGA[4]		930	uA
SPGA[4]		420	uA
DAC buffer		220	uA
DAC		100	uA
Phase Comparator		50	uA
Comparator		60	uA
UART	UART clock 100MHz, 512000 bps	370	uA
SPI	SPI clock 50MHz, 20Mbps	260	uA
PWM	PWM clock 100MHz	1090	uA
ECAP	ECAP clock 100MHz	310	uA
WDT	WDT clock 100MHz	210	uA
TIMER	TIMER clock 100MHz	130	uA
FLASH	HCLK clock 100MHz	320	uA
XO	HCLK is from 100MHz PLL, which takes RCO0 as input	630	uA
RCO0	HCLK is from 100MHz PLL, which takes XO (32MHz) as input	240	uA
PLL	XO (32MHz) as HCLK source, f_{PLL} = 100 MHz	940	uA

[1] For peripherals with multiple instances, the current quoted is for single modules (result of average).

[2] Typical values are measured at TA = 25 °C, VDD = 3.3 V.

[3] ADC analog current contain ADC analog module, bandgap and ADC reference buffer.

[4] The Bandgap must be enabled when enabling ADC (Analog Part), T-sensor, PGA, DAC and comparator.

5.6 Internal 1.2V regulator characteristics

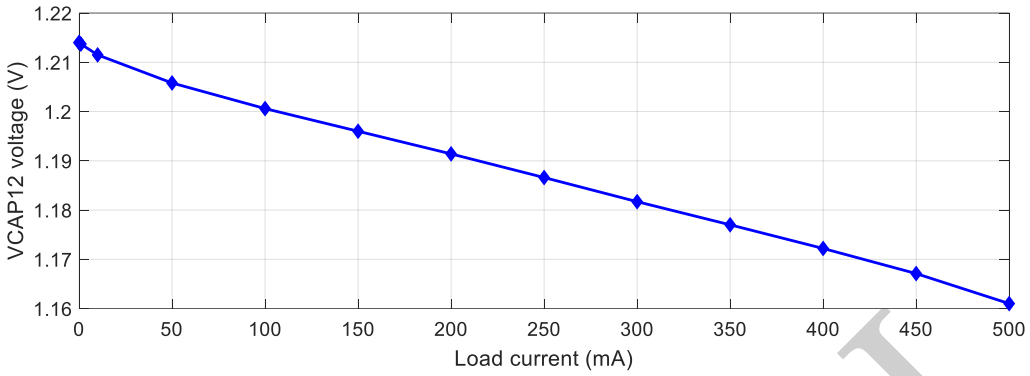
Table 5-10: Internal 1.2V regulator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DVDD33}	3.3V supply voltage	–	2.97	3.3	3.63	V
C_{load}[1]	Load capacitance	–	1	2.2	4.7	uF
I_{load}	Load current (active mode)	–	–	–	40	mA
V_{out_trim}	Calibration step (active mode)	–	–	20	–	mV
V_{out}	Output voltage (active mode)	–	–	1.2	–	V
d_{V_load}	Load regulation ratio (active mode)	–	–	14	40	mV
I_{oc}	Overcurrent threshold (active mode)	–	60	81.5	107	mA
V_{out}[2]	Output voltage (stop mode)	–	–	1.2	–	V

[1] The project is not tested in production, design assurance.

[2] Only internal chip loads can be driven.

Figure 5-2: Internal 1.2V regulator load regulation



5.7 BOD characteristics

Table 5-11: VCAP12 BOD characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{th1(VCAP12OV)}$	VCAP12 overvoltage trigger threshold	–	–	1.33	–	V
$V_{th0(VCAP12OV)}$	VCAP12 overvoltage revocation threshold	–	–	1.31	–	V
$V_{th1(VCAP12UV)}$	VCAP12 undervoltage trigger threshold	–	–	1.1	–	V
$V_{th0(VCAP12UV)}$	VCAP12 undervoltage revocation threshold	–	–	1.14	–	V

Table 5-12: DVDD33 BOD characteristics

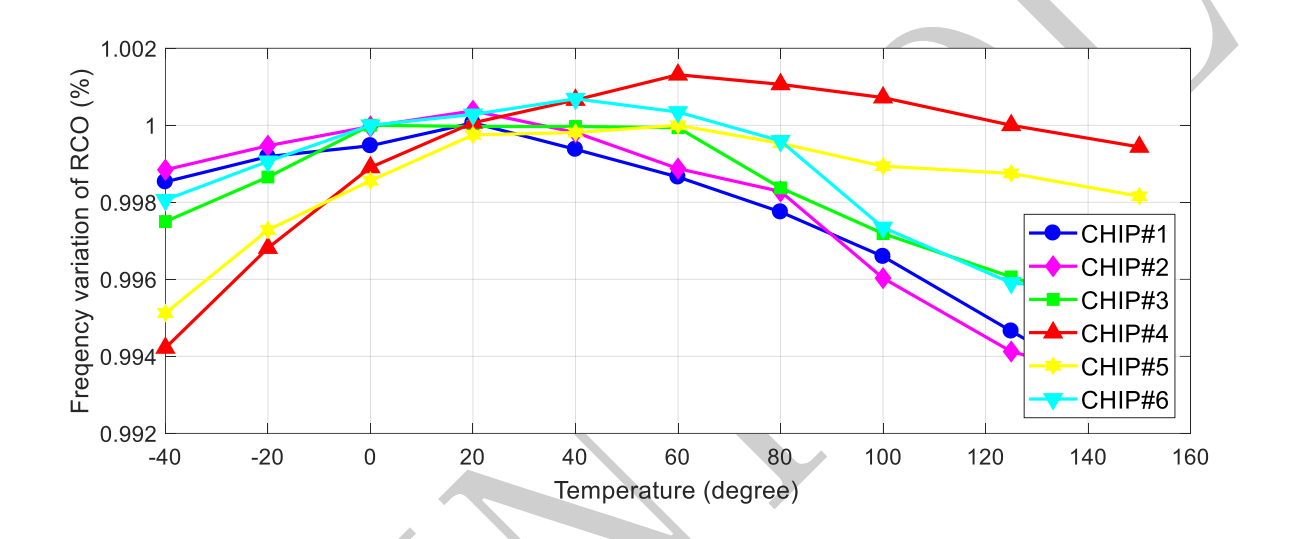
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{th1(DVDD33OV)}$	VDD33 overvoltage trigger threshold	–	–	4.24	–	V
$V_{th0(DVDD33OV)}$	VDD33 overvoltage revocation threshold	–	–	4.08	–	V
$V_{th1(DVDD33UV)}$	VDD33 undervoltage trigger threshold	–	–	2.58	–	V
$V_{th0(DVDD33UV)}$	VDD33 undervoltage revocation threshold	–	–	2.65	–	V

5.8 RCO characteristics

Table 5-13: RCO characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DVDD33}	3.3V power supply	–	2.97	3.3	3.63	V
f_{RCO}	RCO frequency at room temperature	T_J = 25 °C	31.936	–	32.064	MHz
E_{RCO}	RCO frequency accuracy (f_{RCO} variation versus temperature)	T_J = -40~150 °C	-1.5	–	1.5	%
t_{settle}	RCO frequency ready time	–	–	4.2	–	us

Figure 5-3: RCO frequency vs. temperature



5.9 PLL characteristics

Table 5-14: PLL characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DVDD33}	3.3V power supply	–	2.97	3.3	3.63	V
f_{VCO}	VCO frequency	T_J = -40~150 °C	400	500	600	MHz
f_{PFD}[1]	Phase-Frequency Detector (PFD) input frequency	–	4	–	8	MHz
t_{lock}[1]	Locking time	T_J = 25 °C	–	10	15	us
t_{jitter}	PLL output clock jitter	T_J = 25 °C	–	40	–	ps

[1] The project is not tested in production, design assurance.

5.10 XO characteristics

Table 5-15: XO characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DVDD33}	3.3V power supply	–	2.97	3.3	3.63	V
f_{XO}	XO frequency	TJ = -40~150 °C	4	–	32	MHz

5.11 13-bit ADC characteristics

Table 5-16: 13-bit ADC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DVDD33}	Power supply	–	2.97	3.3	3.63	V
N_R	Resolution	No missing code Monotonic	13	–	–	bits
f_S	Conversion speed[1]	–	–	–	2.5	MSPS
V_{in}	Input voltage range	–	0	–	V_{DDA}	V
V_{ref}	Reference voltage	–	1.194	1.2	1.206	V
I_{on}	Operational current	V_{DVDD33} = 3.3 V	–	8.5	11.5	mA
INL	Integral linearity error	–	-3.0	–	3.0	LSB
DNL	Differential linearity	–	-1.0	–	1.0	LSB
E_{offset}	Offset error[2]	With calibration	-4	±2	4	LSB
E_{gain}	Gain error[2]	With calibration	-36	±4	36	LSB
T_{coef}	ADC temperature coefficient with internal reference	–	–	30	–	ppm/°C
t_{settle}[3]	Startup time	–	–	–	100	us
$ENOB_{DC}$	DC Noise Floor	–	–	11.5	–	bits
SNR	Signal-to-noise ratio	f_{in} = 100kHz V_{in} = 0.94FS N = 8192	–	71	–	dB
THD	Total harmonic distortion		–	-84	–	dB
ENOB	Effective number of bits		–	11.4	–	bits
SFDR	Spurious free dynamic range		–	80	–	dB

[1] Sampling time = 200ns, conversion time = 200ns.

[2] Offset and gain can be calibrated automatically by hardware.

[3] The project is not tested in production, design assurance.

5.12 Monitoring ADC characteristics

Table 5-17: Monitoring ADC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DVDD33}	Power supply	–	2.97	3.3	3.63	V
N_R	Resolution	No missing code. Monotonic	13	–	–	bits
f_S	Conversion speed[1]	–	–	–	500	kSPS
V_{in}	Input voltage range	–	0	–	V_{DDA}	V
V_{ref}	Reference voltage	–	1.19	1.2	1.21	V
I_{on}	Operational current	V_{DVDD33} = 3.3 V	–	2.8	3.6	mA
INL	Integral linearity error	–	-3.0	–	3.0	LSB
DNL	Differential linearity	–	-1.0	–	1.0	LSB
E_{offset}	Offset error	With calibration	-4	±2	4	LSB
E_{gain}	Gain error	With calibration	-36	±4	36	LSB
$ENOB_{DC}$	DC Noise Floor	–	–	11.5	–	bits
SNR	Signal-to-noise ratio	f_{in} = 50kHz V_{in} = 0.94FS N = 4096	–	71	–	dB
THD	Total harmonic distortion		–	-84	–	dB
ENOB	Effective number of bits		–	11.4	–	bits
SFDR	Spurious free dynamic range		–	80	–	dB

[1] Sampling time = 1us, conversion time = 1us.

5.13 T-sensor characteristics

Table 5-18: T-sensor characteristics（TBD）

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$TMCU_{slope}$	temperature corresponding to every 1LSB increase of ADC output	–	–	3.808	–	°C/LSB
$TMCU_{offset}$	T-sensor=25 °C, ADC output value	–	–	-81.069	–	LSB

5.14 DPGA characteristics

Table 5-19: DPGA characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DVDD33}	3.3V power supply	–	2.97	3.3	3.63	V
V_{in}	Differential input range	–	-2.7/G	–	+2.7/G	V
V_{OUT}	Output voltage range	–	0.3	–	V_{DVDD33}-0.3	V
R_{IN}	Input impedance	–	–	4	–	kΩ
G	Gain	Differential	2/4/8/16/24/32/48/64			–
E_{gain}	Gain error	Differential Gain = 2	-1	–	1	%
		Differential Gain=16	-1	–	1	%
		Differential Gain = 64	-1	–	1	%
V_{Offset}	Offset	Differential Gain=2	-3	–	3	mV
		Differential Gain=16	-1.3	–	+1.3	mV
		Differential Gain=64	-1	–	+1	mV
V_{CM}	Common mode input voltage range	Differential Gain=2	-1.5	–	2	V
		Differential Gain=4	-0.9	–	2	V
		Differential Gain=8	-0.75	–	2	V
		Differential Gain=16	-0.6	–	2	V
		Differential Gain=24	-0.57	–	2	V
		Differential Gain=32	-0.55	–	2	V
		Differential Gain=48	-0.52	–	2	V
		Differential Gain=64	-0.5	–	2	V
t_{settle}	Settle time[1]	Differential Gain=2	–	313.7	441.6	ns
		Differential Gain=4	–	303.1	425.5	ns
		Differential Gain=8	–	268.4	423.8	ns
		Differential Gain=16	–	376.7	604.7	ns
		Differential Gain=24	–	355.8	598.9	ns
		Differential Gain=32	–	442.9	742.3	ns
		Differential Gain=48	–	628.0	1061.0	ns
		Differential Gain=64	–	813.3	1378.0	ns
GBW	Gain bandwidth[2]	Differential gain = 2	6	9.68	–	MHz
		Differential gain = 4	3.8	6.07	–	MHz
		Differential gain = 8	2.56	3.45	–	MHz
		Differential gain = 16	1.37	1.85	–	MHz
		Differential gain = 24	1.23	1.63	–	MHz
		Differential gain = 32	0.93	1.23	–	MHz
		Differential gain = 48	0.63	0.83	–	MHz
		Differential gain = 64	0.4	0.63	–	MHz
SR	Slew rate[3]	Differential gain = 2	15	21	30	V/us
		Differential gain = 4	15	21	30	V/us
		Differential gain = 8	14.5	21	30	V/us
		Differential gain = 16	11.2	18.9	29.7	V/us
		Differential gain = 24	12.57	21	33.4	V/us

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Differential gain = 32	9.25	18.4	31.8	V/us
		Differential gain = 48	6.1	11.5	25	V/us
		Differential gain = 64	4.6	8.6	17.6	V/us
$ENOB_{DC}$	Effective number of bits	Differential Gain = 2	–	11.93	–	bits
		Differential Gain = 16	–	11.57	–	bits
		Differential Gain = 64	–	10.94	–	bits
SNR	Signal-to-noise ratio at 10kHz input	Differential Gain = 2	–	72.2	–	dB
		Differential Gain = 16	–	71.1	–	dB
		Differential Gain = 64	–	64.8	–	dB
THD	Total harmonic distortion at 10kHz input	Differential Gain = 2	–	79.59	–	dB
		Differential Gain = 16	–	81.29	–	dB
		Differential Gain = 64	–	78.47	–	dB
$CMRR_{DC}$	DC common mode rejection Ratio	Differential Gain = 2	–	-59.7	–	dB
		Differential Gain = 16	–	-52.6	–	dB
		Differential Gain = 64	–	-61	–	dB
$PSRR_{DC}$	Power Supply Rejection Ratio	Differential Gain = 2	–	-72.8	–	dB
		Differential Gain = 16	–	-84.9	–	dB
		Differential Gain = 64	–	-93.4	–	dB
I	Current consumption	Differential Gain=2	–	1.215	–	mA
		Differential Gain=16	–	1.096	–	mA
		Differential Gain=64	–	1.152	–	mA

[1] Settle time is measured by step input, and differential output change from -2.7V to 2.7V (VDDA=3.3V), the time for output to be settled to 98%, guarantee by design.

[2] GBW data is guaranteed by design.

[3] Slew rate data is from 10% to 90% of output signal, guaranteed by design.

Figure 5-4: Settling time with different gain

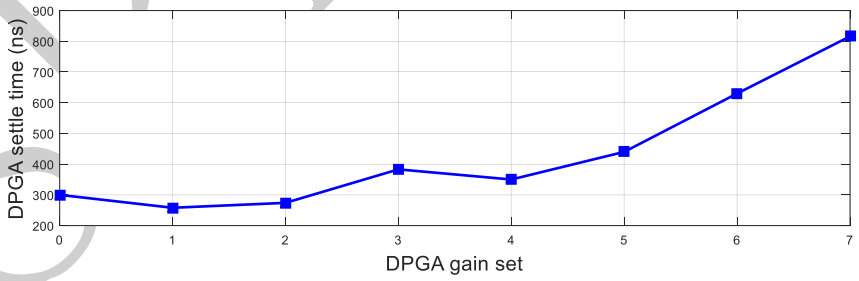


Figure 5-5: ENOB_DC with different gain

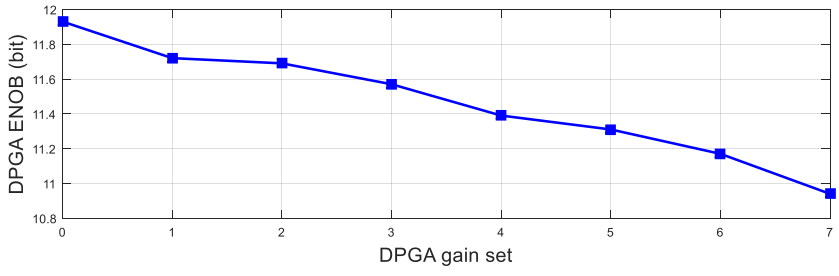


Figure 5-6: SNR with different gain

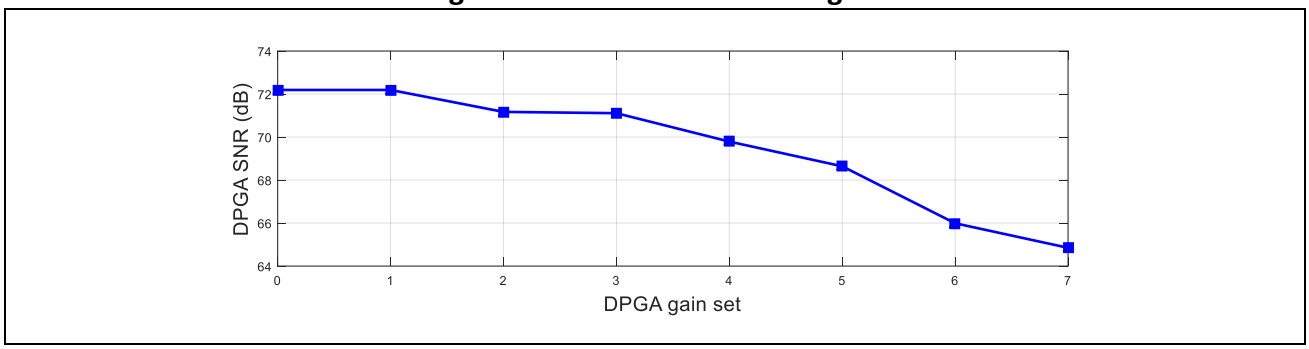


Figure 5-7: THD with different gain

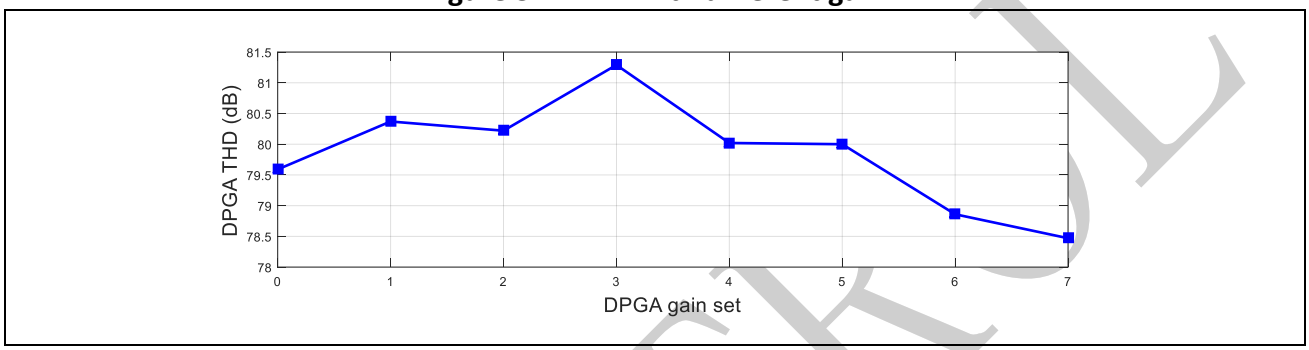


Figure 5-8: CMRR_DC with different gain

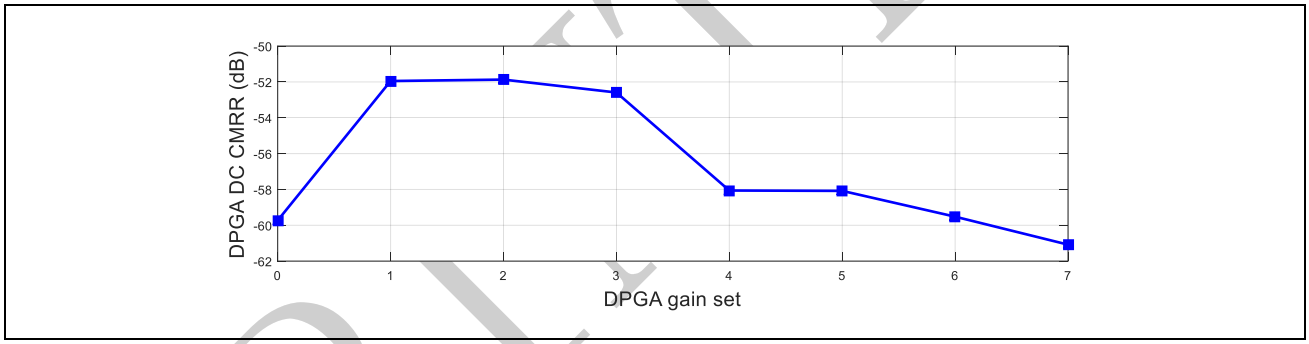
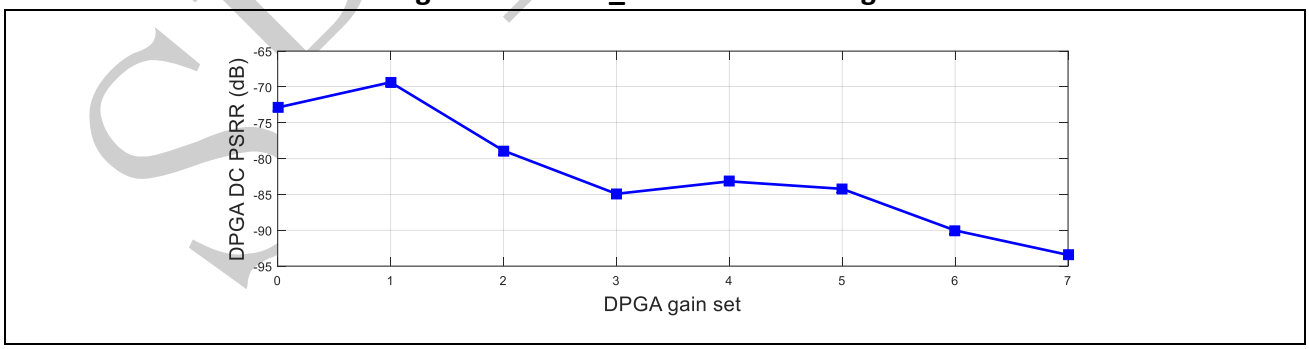


Figure 5-9: PSRR_DC with different gain



5.15 SPGA characteristics

Table 5-20: SPGA characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DVDD33}	Power supply	–	2.97	3.3	3.63	V
V_{in}	Input range	–	0.3	–	V_{DDA}-1.3	V
V_{out}	Output voltage range	–	0.3	–	V_{DDA}-0.3	V
R_{in}	Input impedance	–	–	High-Z	–	Ω
G	Gain	Single-ended	1/2/4/8/16/32/48/64			–
E_{gain}	Gain error	Gain = 2	-1	–	1	%
		Gain = 32	-1	–	1	%
		Gain = 64	-2	–	2	%
V_{offset}	Offset	–	-5	–	5	mV
t_{settle}	Settle time	Gain = 2	–	300	–	ns
		Gain = 32	–	1000	–	ns
		Gain = 64	–	2000	–	ns
ENOB	Effective number of bits	Gain = 2	–	11	–	bits
		Gain = 32	–	9	–	bits
		Gain = 64	–	8	–	bits
I_{on}	Current consumption	–	–	0.5	–	mA

Figure 5-10: Settling time with different gain (TBD)

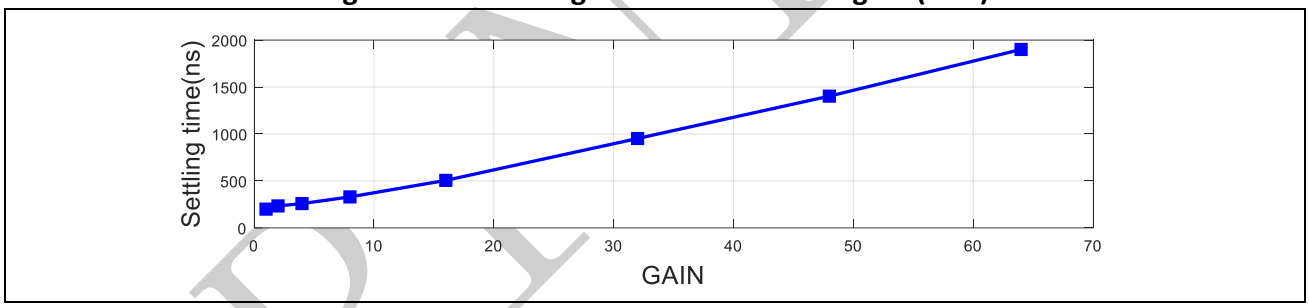
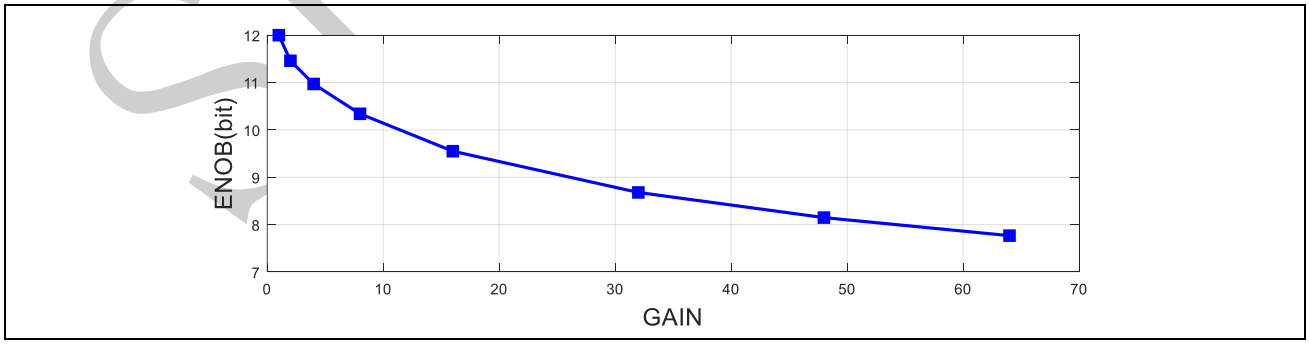


Figure 5-11: ENOB_DC with different gain (TBD)



5.16 Analog comparator characteristics

Table 5-21: Analog omparator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DVDD33}	3.3V supply voltage	–	2.97	3.3	3.63	V
V_{in}	Input voltage range	–	0	–	V_{DVDD33}	V
V_{offset}	Offset voltage(Hysteresis voltage=0)	V_{DVDD33}=3.3V T_J = 25°C V_{cm} = 1.65V	-5	–	5	mV
V_{hyst}	Hysteresis voltage(0mV)		–	0	–	mV
	Hysteresis voltage(12mV)		–	13	–	mV
	Hysteresis voltage(24mV)		–	25	–	mV
	Hysteresis voltage(36mV)		–	37	–	mV
t_d	Delay time – comparator response time to PWM shunt down (Asynchronous)		–	50	–	ns

5.17 Phase comparator characteristics

Table 5-22: Phase comparator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DVDD33}	3.3V supply voltage	–	2.97	3.3	3.63	V
V_{in}	Input voltage range	–	0	–	V_{DVDD33}	V
V_{offset}	Offset voltage (Hysteresis voltage=0)	V_{DVDD33} = 3.3V T_J = 25°C V_{cm} = 1.65V	-3.5	–	3.5	mV
V_{hyst}	Hysteresis voltage option = 0		–	0	–	mV
	Hysteresis voltage option = 1		–	13	–	mV
	Hysteresis voltage option = 2		–	25	–	mV
	Hysteresis voltage option = 3		–	37	–	mV
t_d	Delay time – comparator response time to PWM shunt down (Asynchronous)		–	250	–	ns

5.18 Internal 10-bit DAC characteristics

Table 5-23: DAC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DVDD33}	3.3V supply voltage	–	2.97	3.3	3.63	V
N	resolution	Monotonic	10	–	–	bit
V_{FS}	Full scale value	–	0	–	V_{DVDD33}	V
DNL	Differential linearity	–	-0.5	–	0.5	LSB
INL	Integral linearity	–	-1	–	1	LSB
E_{offset}	Offset error	–	–	5	–	mV
t_{settle}	DAC settling time	Design guarantee	–	–	1	us

[1] The DAC is used to generate a static voltage as the threshold of the comparator and does not guarantee the performance of dynamically changing the code value to generate the waveform.

Figure 5-12: DNL curve

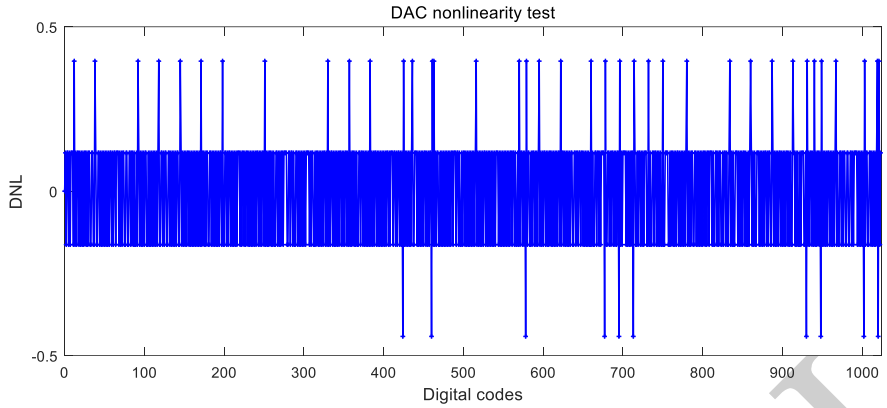
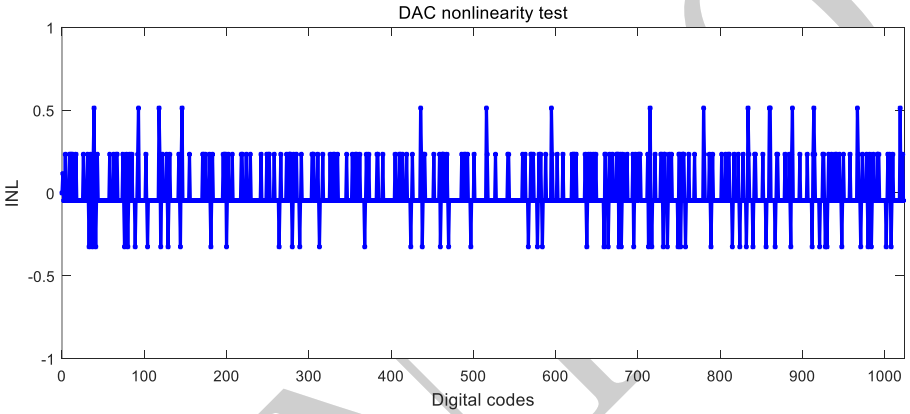


Figure 5-13: INL curve

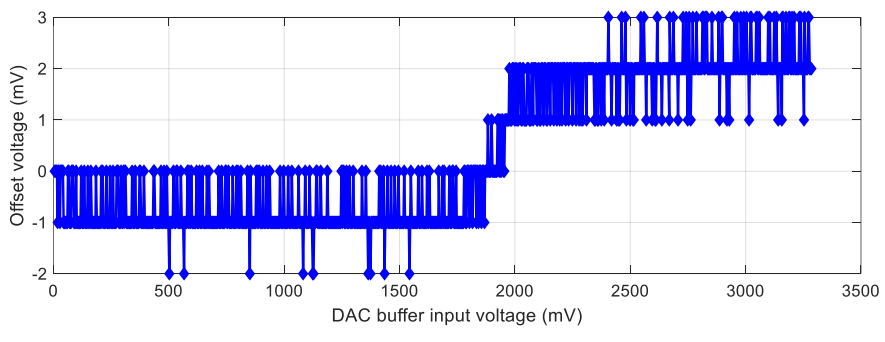


5.19 DAC buffer characteristics

Table 5-24: DAC buffer characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DVDD33}	Power supply	–	2.97	3.3	3.63	V
V_{out}	Output voltage range	–	0.3	–	V_{DVDD33}-0.4	V
t_{settle}	Settling time	Design guarantee	–	1	–	us
E_{offset}	Offset error	–	–	5	–	mV
C_L	Capacitor load	Design guarantee	–	–	50	pF
R_L	Resistor load	Design guarantee	5k	–	–	Ω

Figure 5-14: DAC buffer offset over Input voltage



5.20 D2S buffer characteristics

Table 5-25: D2S buffer characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DVDD33}	Power supply	–	2.97	3.3	3.63	V
V_{out}	Output voltage range	–	0.3	–	V_{DDA} - 0.3	V
t_{settle}	Settling time[1]	Design guarantee	–	10	–	ms
E_{offset}	Offset error	–	–	10	–	mV
E_{gain}	Gain error	–	–	1	–	%
C_L	Capacitor load	–	–	1	–	uF
I_{on}	Current consumption	–	–	1	–	mA

[1] Settling time is measured by adding external RC filter, typical value is R=1K, C=1uF.

5.21 Flash memory characteristics

The characteristics are given at T_J = -40 to 150 °C unless otherwise specified.

Table 5-26: Flash memory characteristics

Symbol	Parameter	Condition	Min	Max	Unit
t_{RD}	Read access time	–	35	–	ns
t_{PROG}	Word (64-bit) program time	–	8	10	us
t_{SE}	Sector erase time	–	3.2	4	ms
t_{CE}	Chip erase time	–	16	20	ms
N_{END}	Endurance (erase/program cycle)	T_J = 85 °C	100000	–	cycles
t_{RET}	Data retention duration	T_J = 85 °C	20	–	years

5.22 SPI characteristics

Table 5-27: SPI characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency	–	–	–	50	MHz
$t_{SCLK(H)}$	SCLK clock high time	–	10	–	–	ns
$t_{SCLK(L)}$	SCLK clock low time	–	10	–	–	ns
SPI master mode						
$t_{V(MO)}$	Data output valid time	–	–	–	9.5	ns
$t_{H(MO)}$	Data output hold time	–	3.9	–	–	ns
$t_{SU(MI)}$	Data input setup time	–	6	–	–	ns
$t_{H(MI)}$	Data input hold time	–	2	–	–	ns
SPI slave mode						
$t_{SU(SFRM)}$	SFRM enable setup time	–	5.6	–	–	ns
$t_{H(SFRM)}$	SFRM enable hold time	–	1.5	–	–	ns
$t_{A(SO)}$	Data output access time	–	4	–	10	ns
$t_{DIS(SO)}$	Data output disable time	–	4	–	10	ns
$t_{V(SO)}$	Data output valid time	–	-	–	9.5	ns
$t_{H(SO)}$	Data output hold time	–	3.9	–	–	ns
$t_{SU(SI)}$	Data input setup time	–	6	–	–	ns
$t_{H(SI)}$	Data input hold time	–	2	–	–	ns

5.23 Electrical sensitivity characteristics

Table 5-28: ESD absolute maximum ratings

Symbol	Parameter	Condition		Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	Ambient temperature T_A = 25 °C		2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge Device Model)	Ambient temperature T_A = 25 °C	–	500	V
			Corner Pin	750	V

Table 5-29: Electrical sensitivities

Symbol	Parameter	Condition	Max	Unit
LU	Static latch-up	Ambient temperature T_A = 125 °C V_{DD} = 3.63V, V_{CAP12} = 1.32V	100	mA

5.24 Moisture Sensitivity Level characteristics

Table 5-30: Thermal resistance characteristics（QFN48 package）

Symbol	Parameter	Condition	Max	Unit
MSL	Moisture Sensitivity Level	–	3	–

5.25 Thermal resistance characteristics

Table 5-31: Thermal resistance characteristics (LQFP48 package) (TBD)

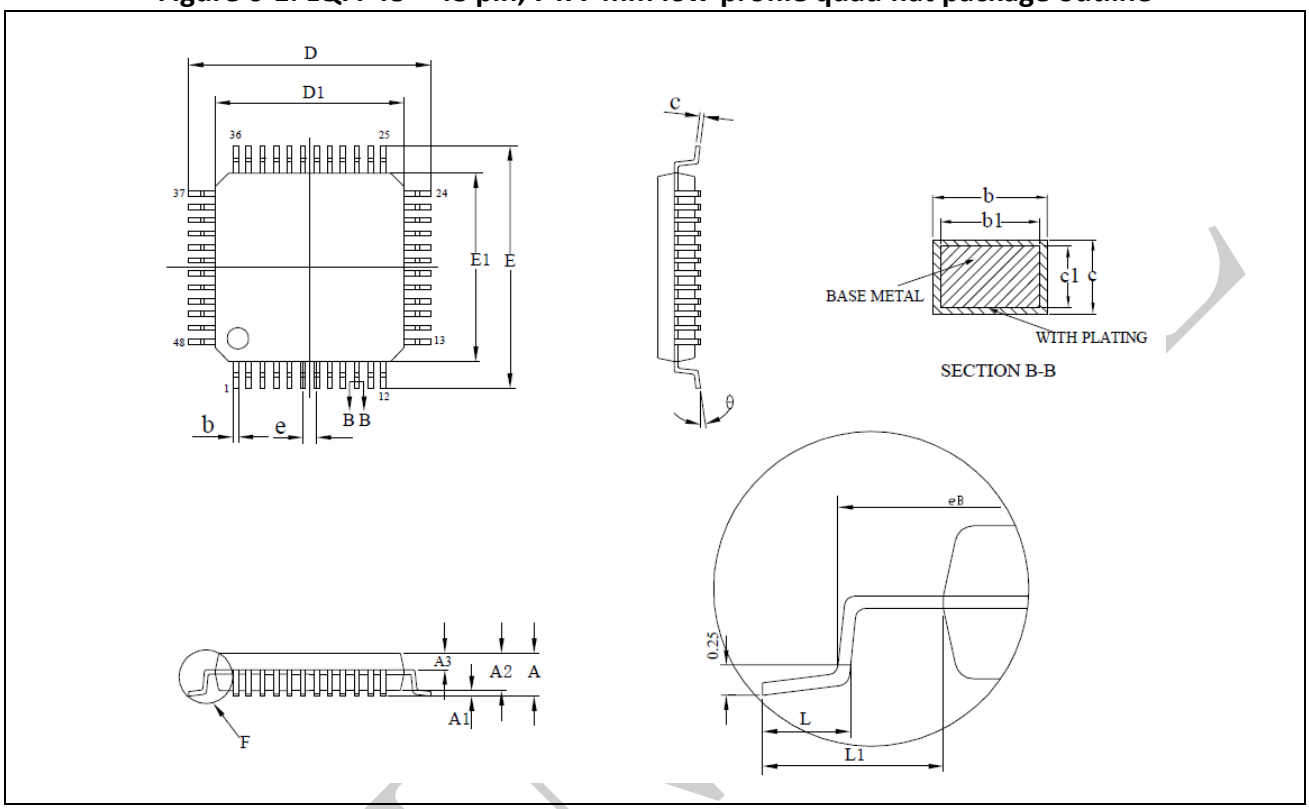
Symbol	Parameter	Condition	Typ	Unit
θ_{JC}	Junction-to-case thermal resistance	–	16.8386	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	Single layer PCB PCB Copper content = 20%	72.1462	°C/W
		4-layer PCB PCB Copper content Top layer = 20%, Second/Third layer = 100%, Bottom layer = 5%	52.3661	°C/W

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

6 Package information

The package type of SPC1169 is 48-pin low-profile quad flat package (LQFP48). The detail information is as follows:

Figure 6-1: LQFP48 – 48 pin, 7 x 7 mm low-profile quad flat package outline



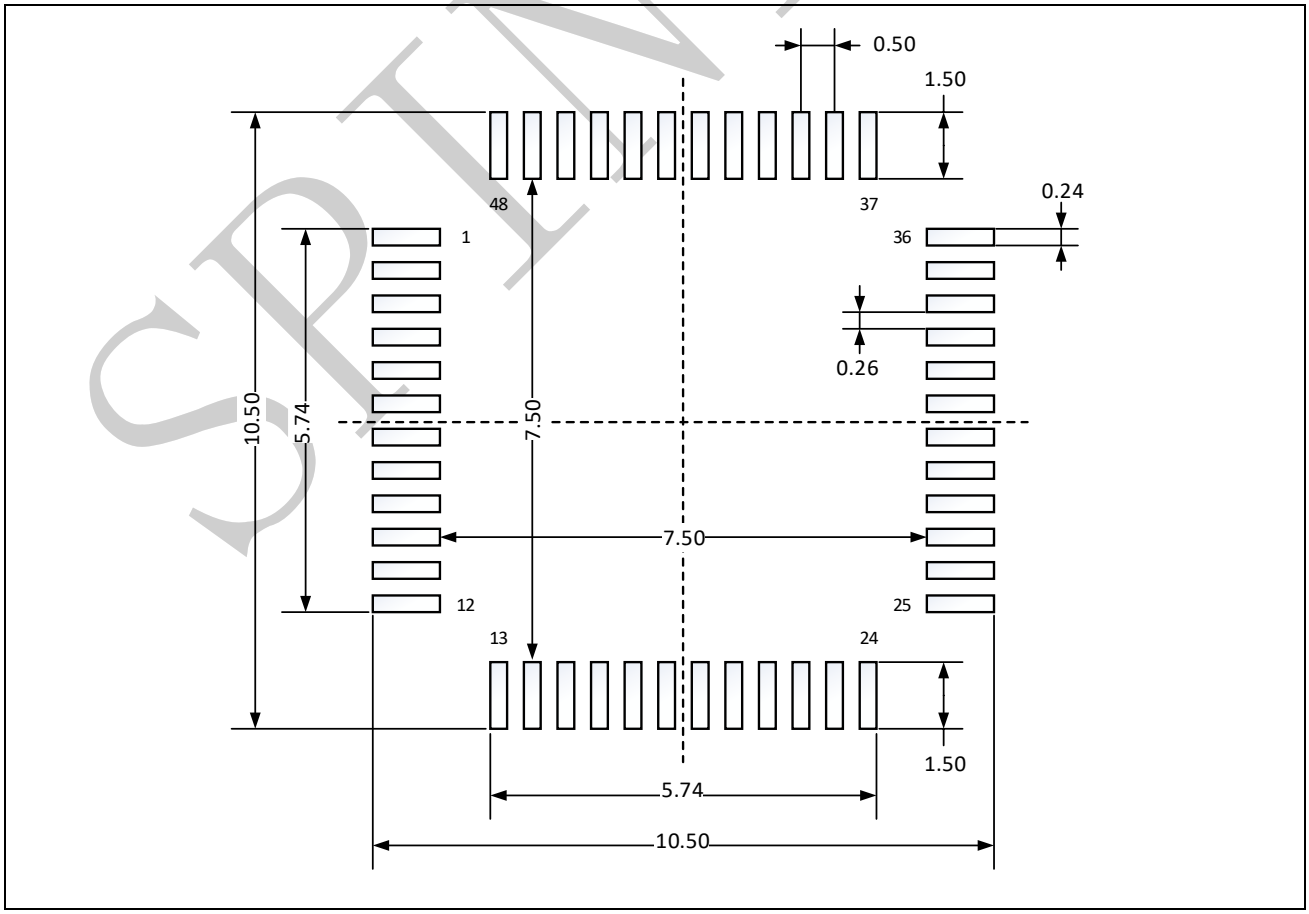
[1] Drawing is not to scale.

Table 6-1: LQFP48 – 48 pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	–	–	1.60	–	–	0.0630
A1	0.05	–	0.15	0.0020	–	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
A3	0.59	0.64	0.69	0.0232	0.0252	0.0272
b	0.18	–	0.26	0.0071	–	0.0102
b1	0.17	0.20	0.23	0.0067	0.0079	0.0091
c	0.13	–	0.17	0.0051	–	0.0067
c1	0.12	0.13	0.14	0.0047	0.0051	0.0055
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.90	7.00	7.10	0.2717	0.2756	0.2795
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.90	7.00	7.10	0.2717	0.2756	0.2795
Eb	8.10	–	8.25	0.3189	–	0.3248
e	–	0.5	–	–	0.0197	–
L	0.4	–	0.75	0.0157	–	0.0295
L1	–	1.00	–	–	0.0394	–
θ	0	–	7°	0	–	7°

[1] Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 6-2: LQFP48 – 48 pin, 7 x 7 mm low-profile quad flat package recommended footprint



[1] Dimensions are expressed in millimeters.

7 Ordering information

Table 7-1: Ordering information

Ordering Number	Flash	SRAM	Max f_{CPU}	Package	Grade	SPQ[1]	Packing
SPC1169DPE48	128KB	32KB	100MHz	LQFP48	AEC-Q100 Grade 1 -40 °C ~ +150 °C	2500	Tray

[1] SPQ = Standard Pack Quantity.

7.1 Rule of ordering number

Figure 7-1: Rule of ordering number